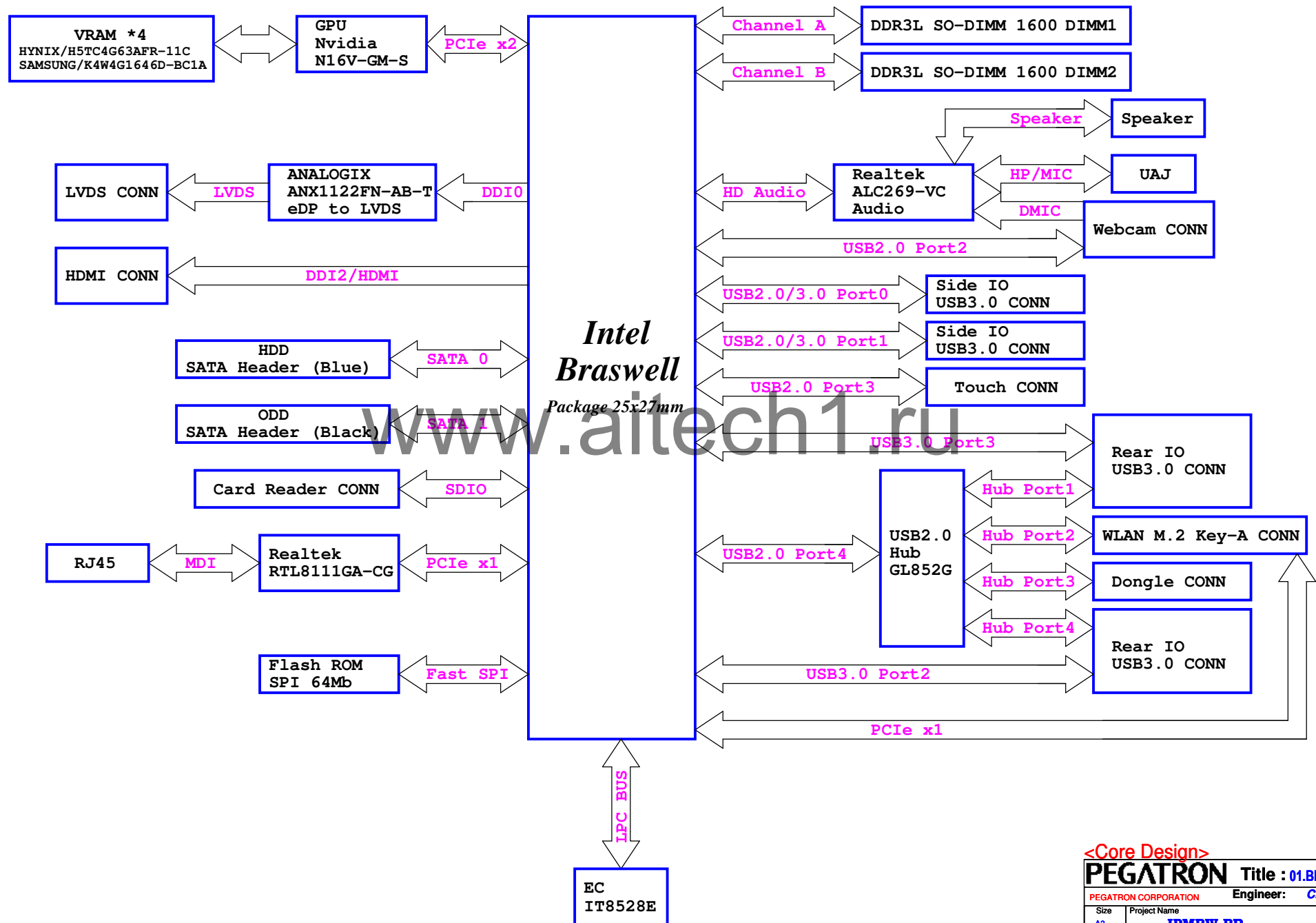


IPMBW-BR



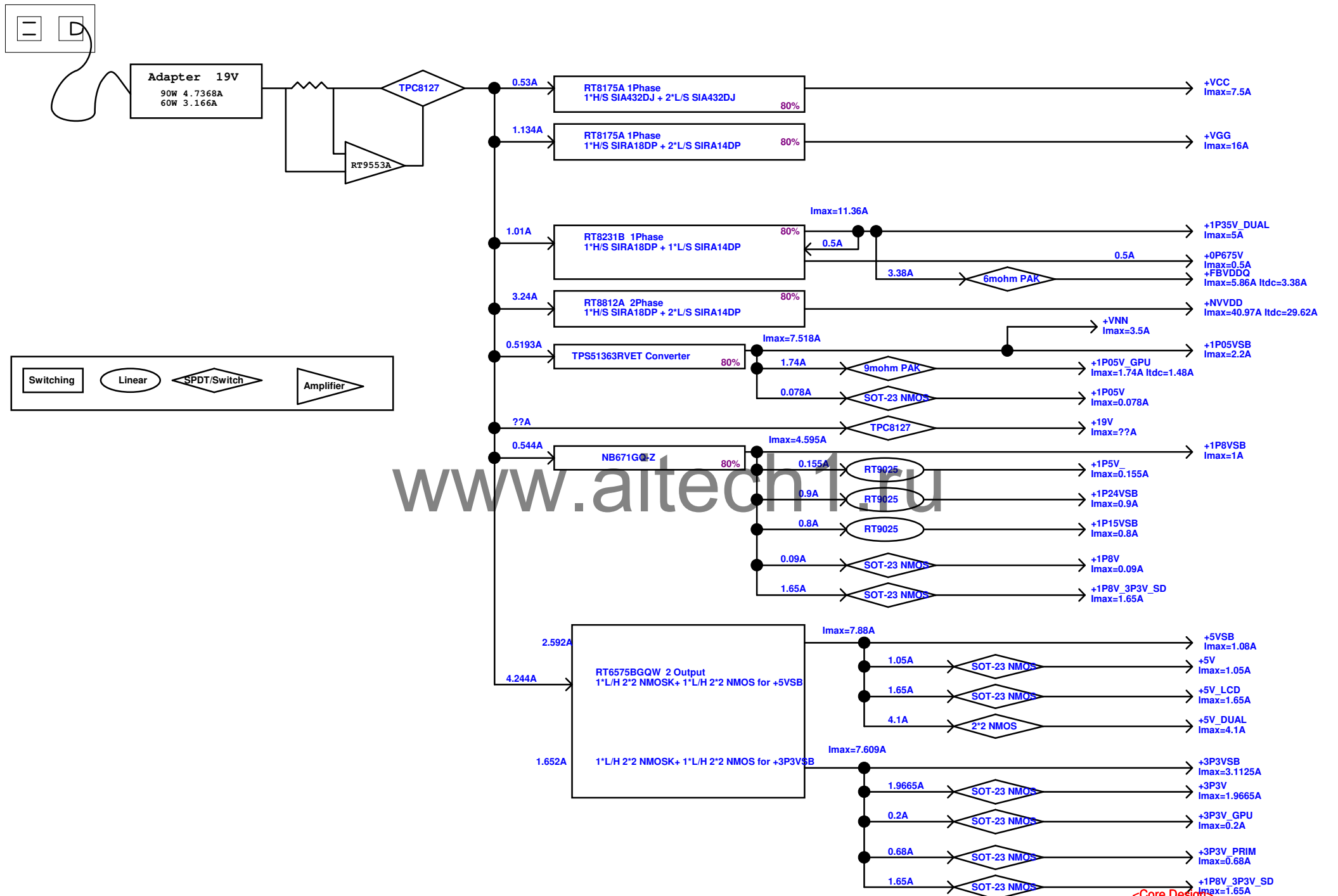
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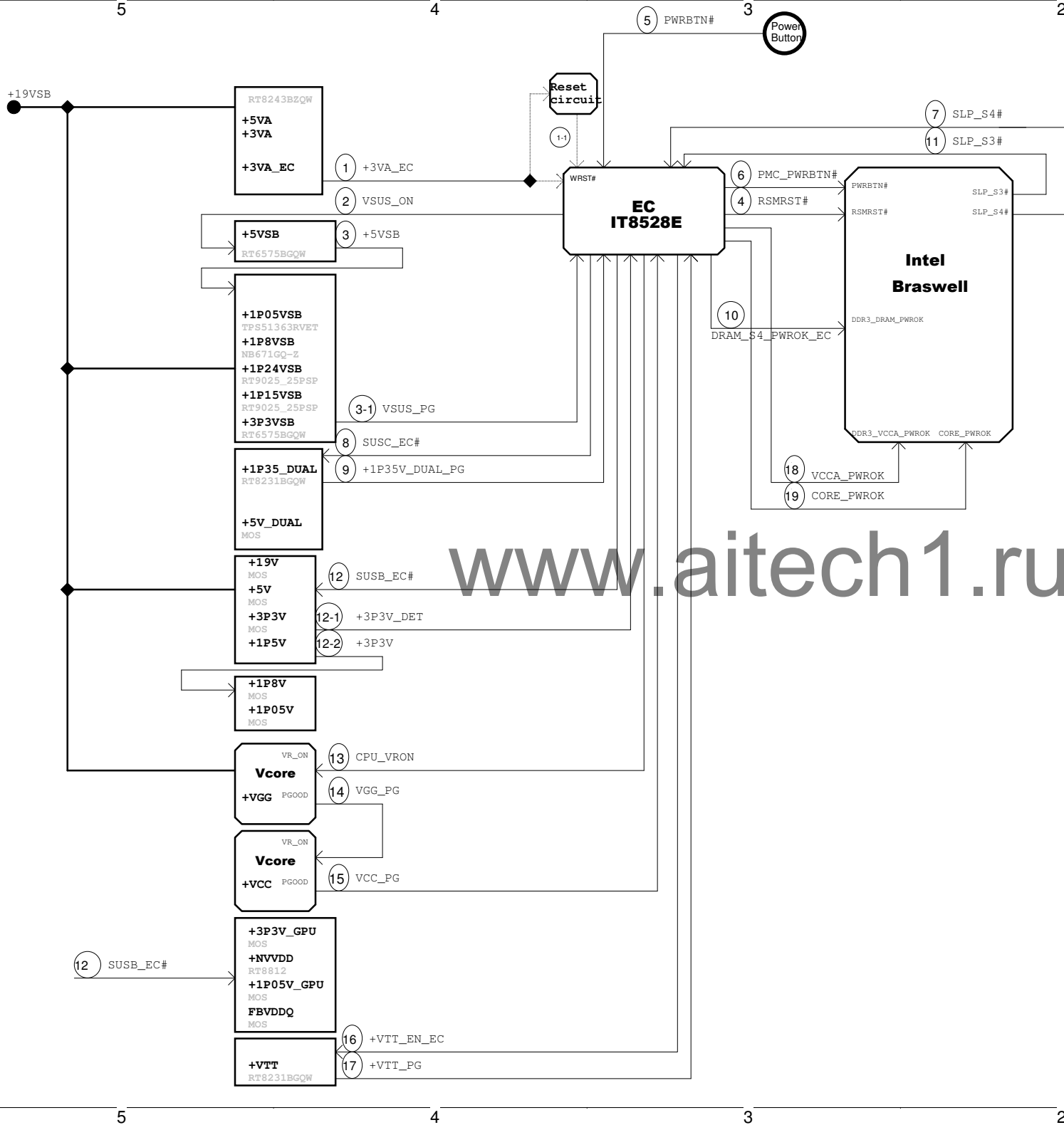
www.aitech1.ru

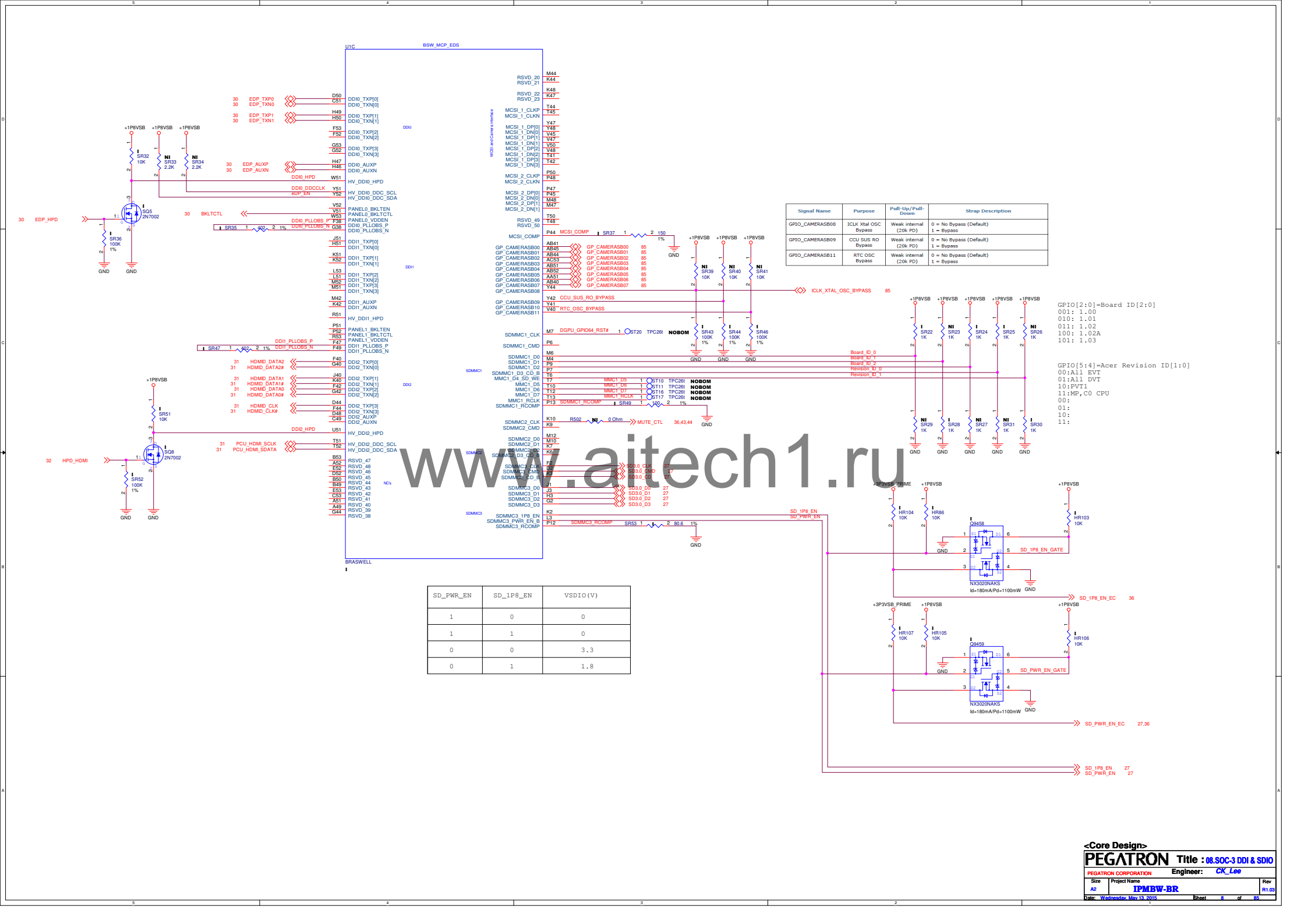
Schematics Change History

Version	Date	Comments
www.aitech1.ru		



www.aitech1.ru

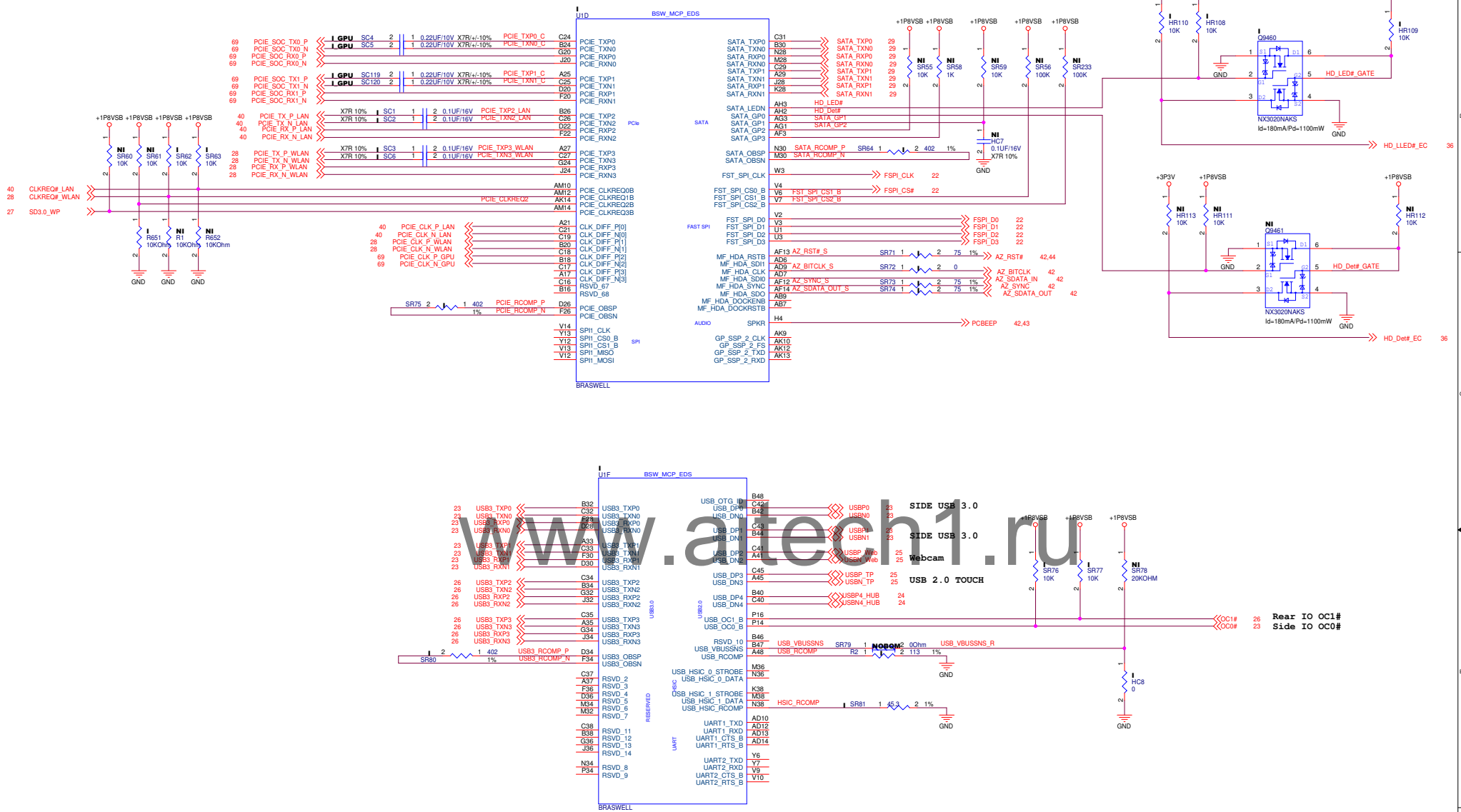


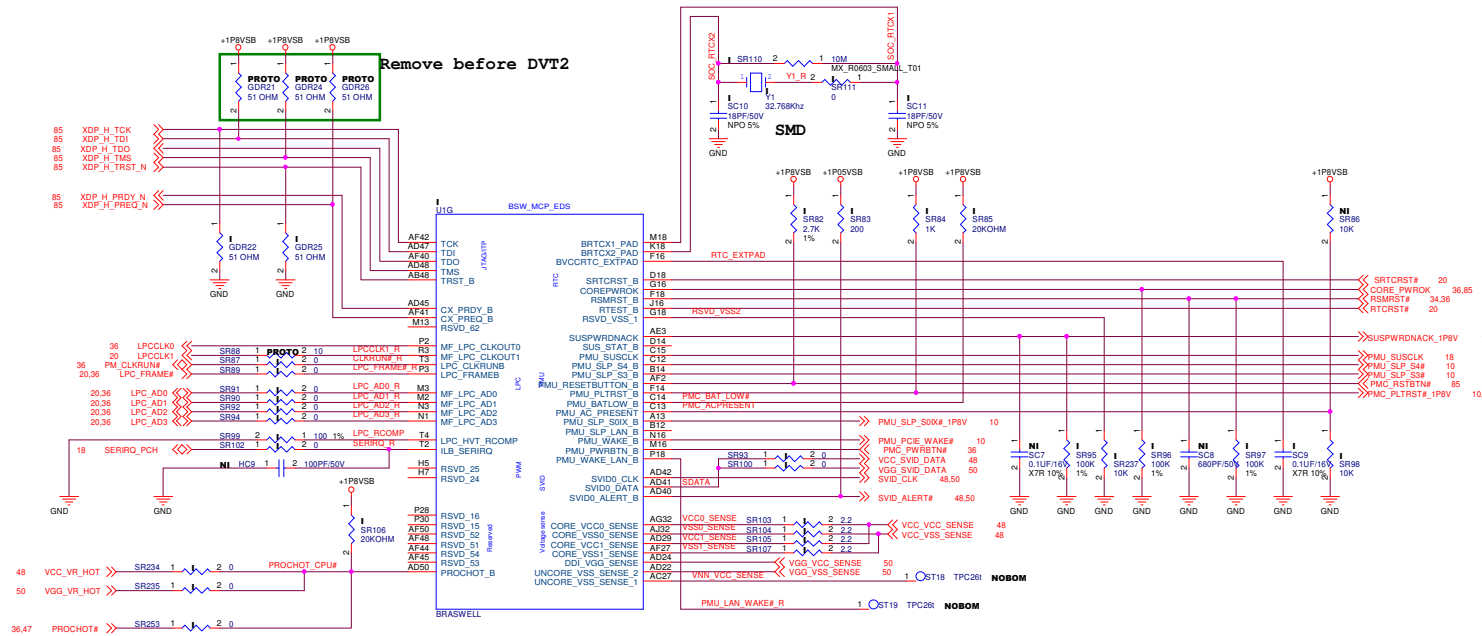


Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_CAMERASB08	ICLK Xtal OSC Bypass	Weak internal (20k PD)	0 = No Bypass (Default) 1 = Bypass
GPIO_CAMERASB09	CCU SUS RO Bypass	Weak internal (20k PD)	0 = No Bypass (Default) 1 = Bypass
GPIO_CAMERASB11	RTC OSC Bypass	Weak internal (20k PD)	0 = No Bypass (Default) 1 = Bypass

GPIO[2:0]=Board ID[2:0]
001: 1.00
010: 1.01
011: 1.02
100: 1.02A
101: 1.03

GPIO[5:4]=Acer Revision ID[1:0]
00:All EVT
01:All DVT
10:PVT1
11:MP,C0 CPU
00:
01:
10:
11:

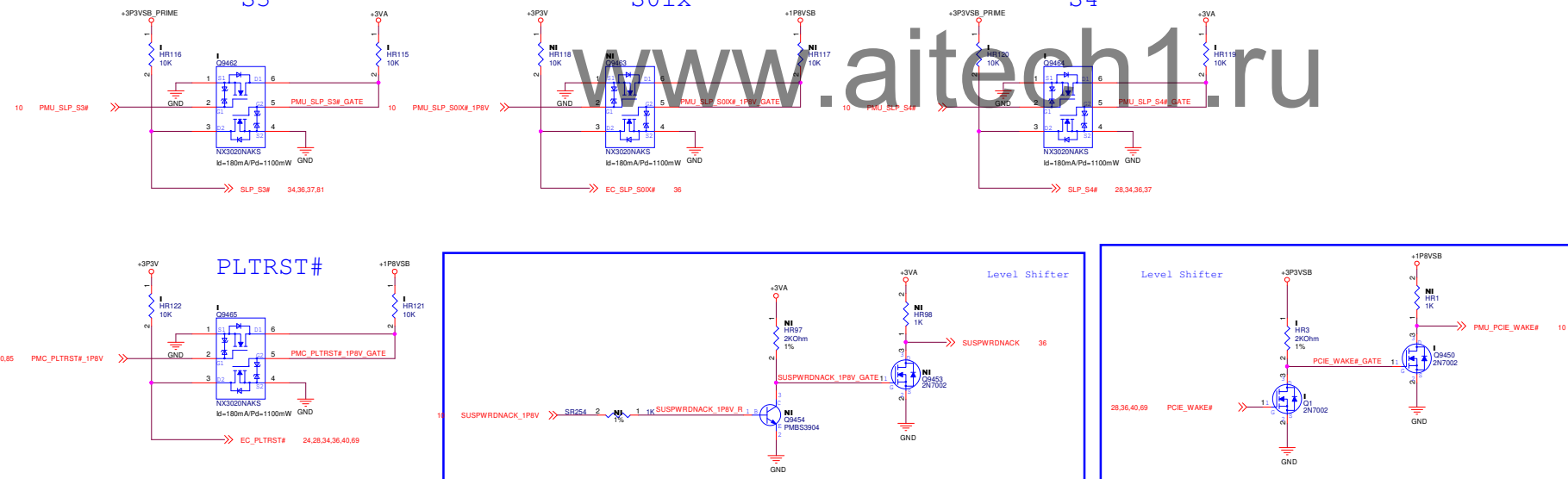




S3

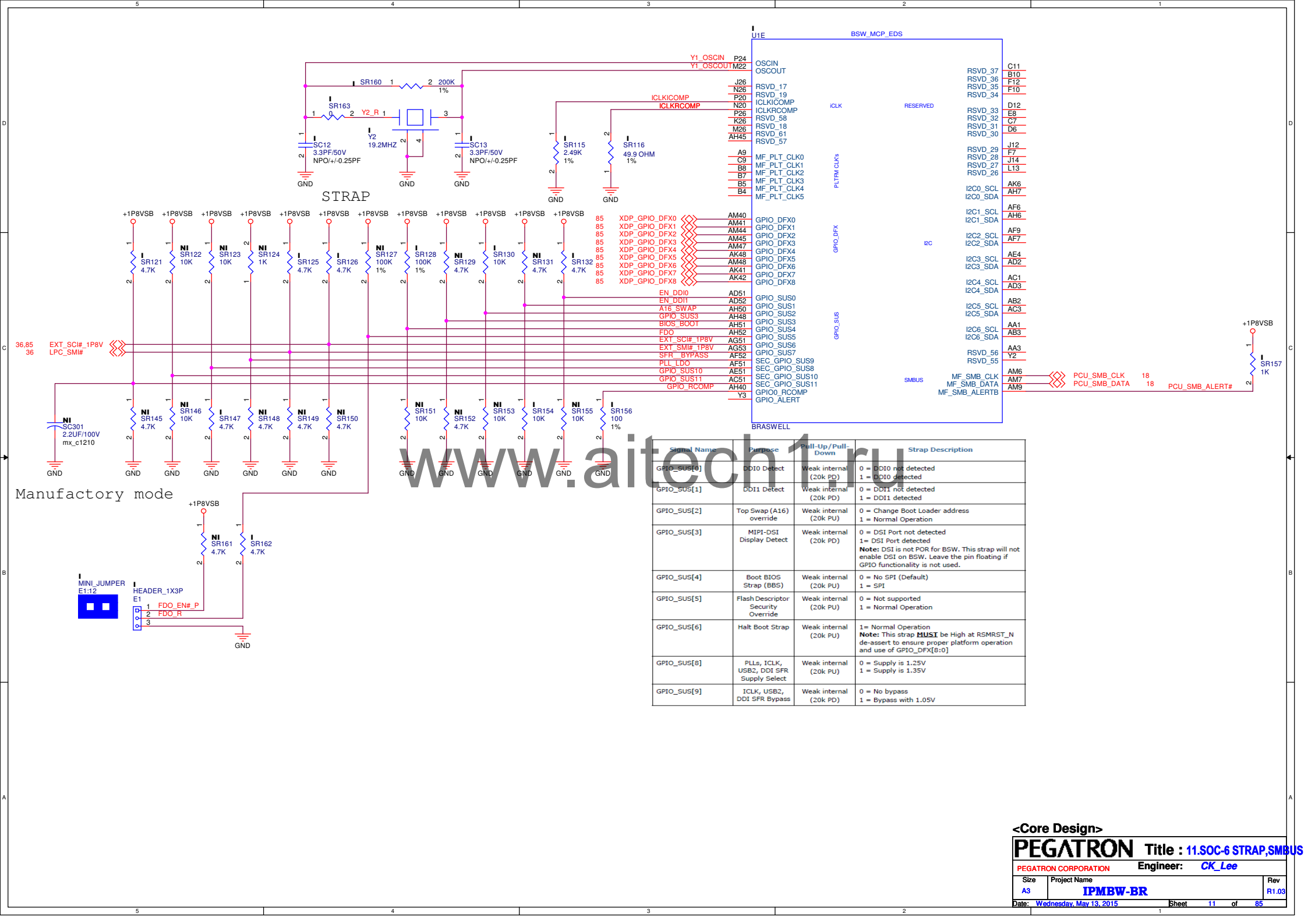
S0ix

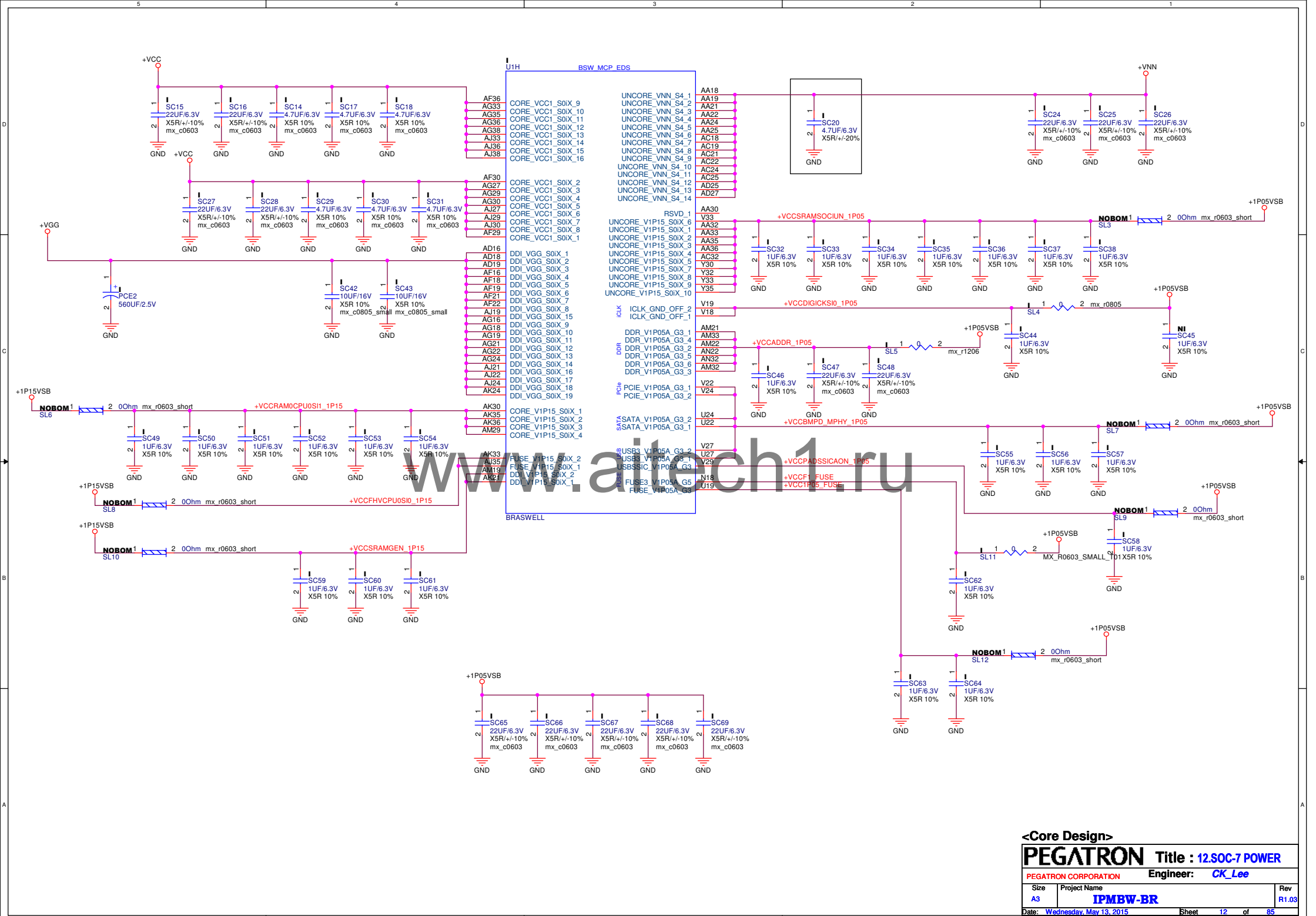
S4

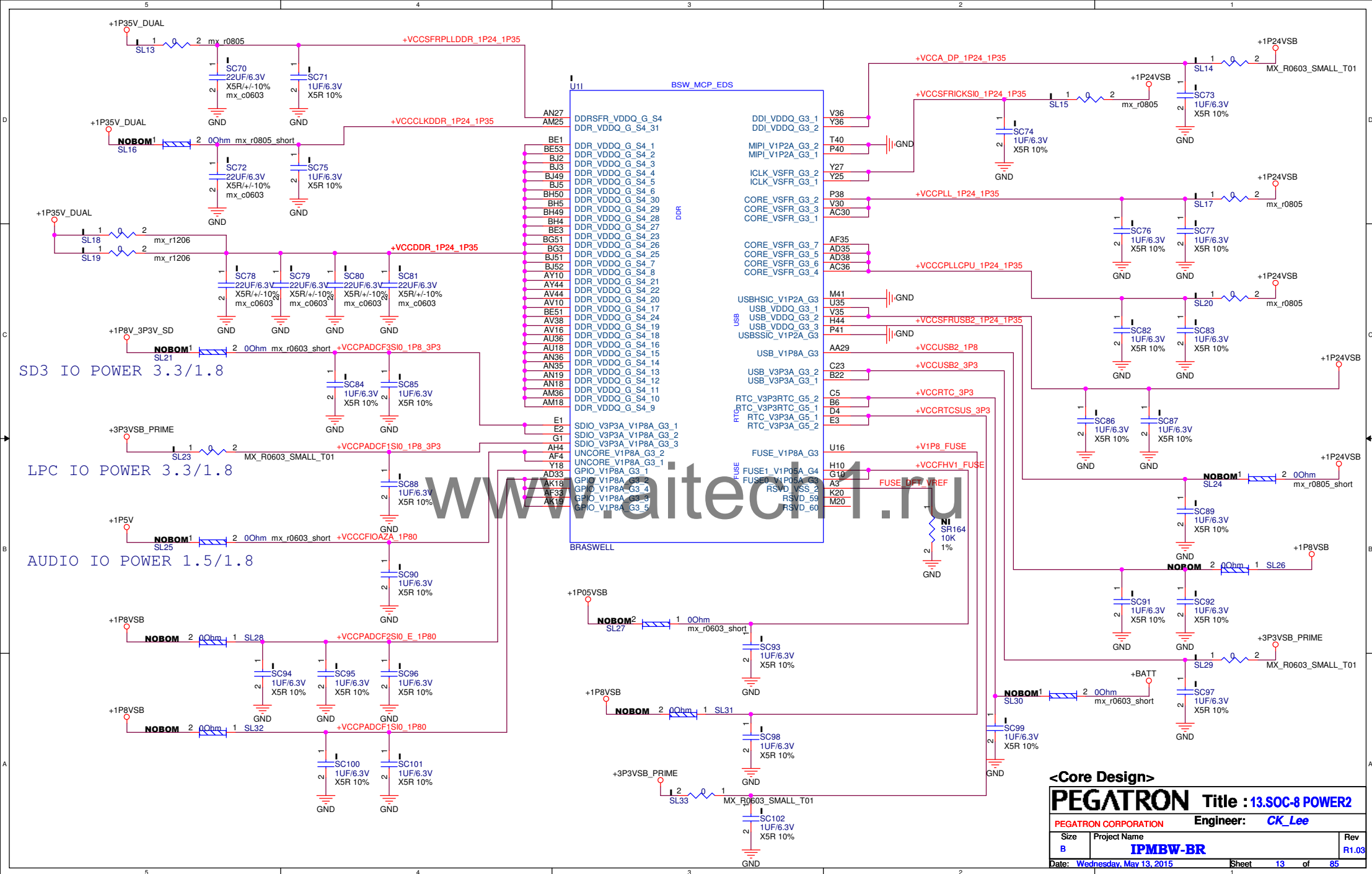


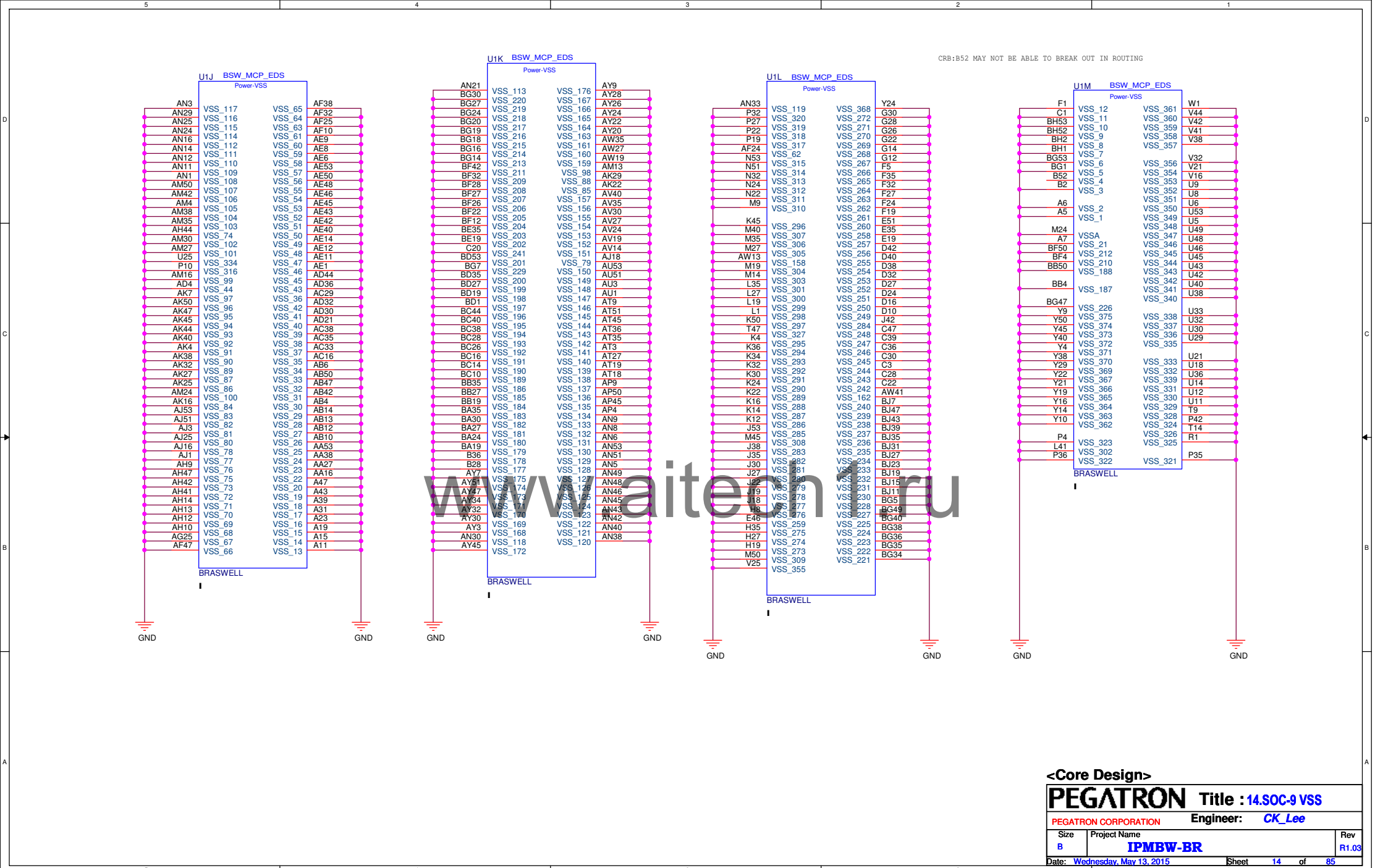
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PEGATRON Title : 10.SOC-5 LPC Sequence			
PEGATRON CORPORATION		Engineer: CK_Lee	
Size	Project Name	Rev	
A2	IPMBW-BR	R1.03	
Date: Wednesday, May 13, 2015		Sheet 10 of 85	









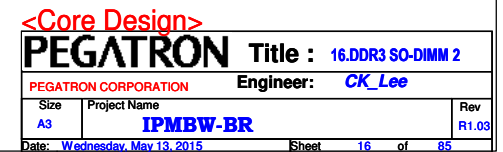
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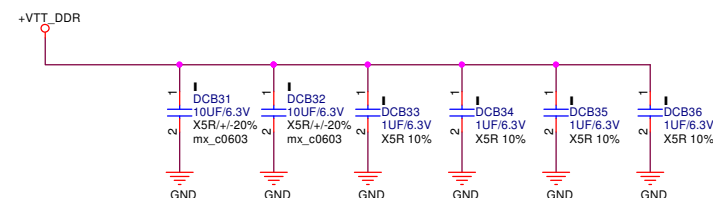
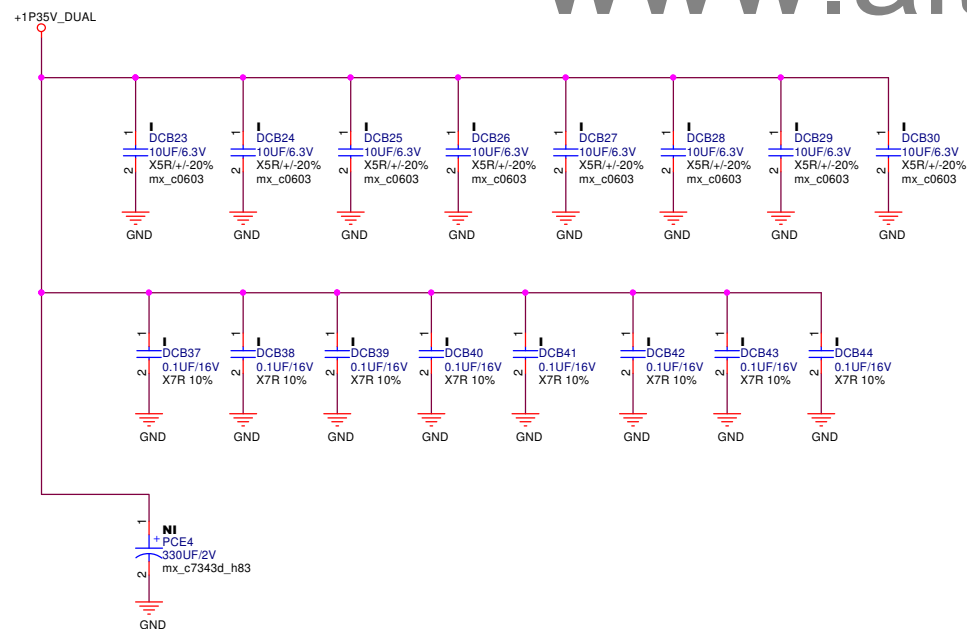
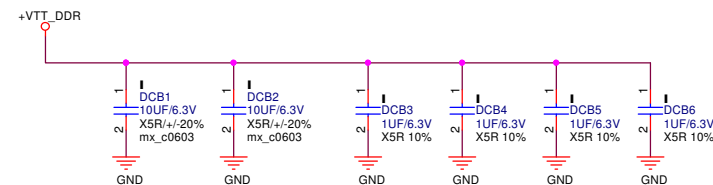
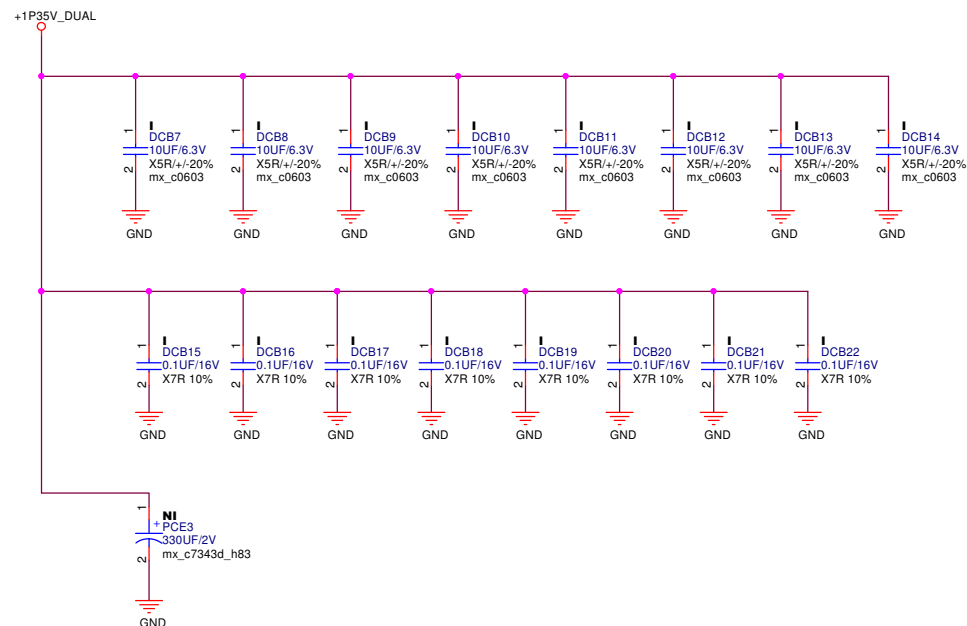
PEGATRON Title : 14.SOC-9 VSS

PEGATRON CORPORATION Engineer: CK_Lee

Size Project Name Rev
B IPMBW-BR R1.03

Date: Wednesday, May 13, 2015 Sheet 14 of 85





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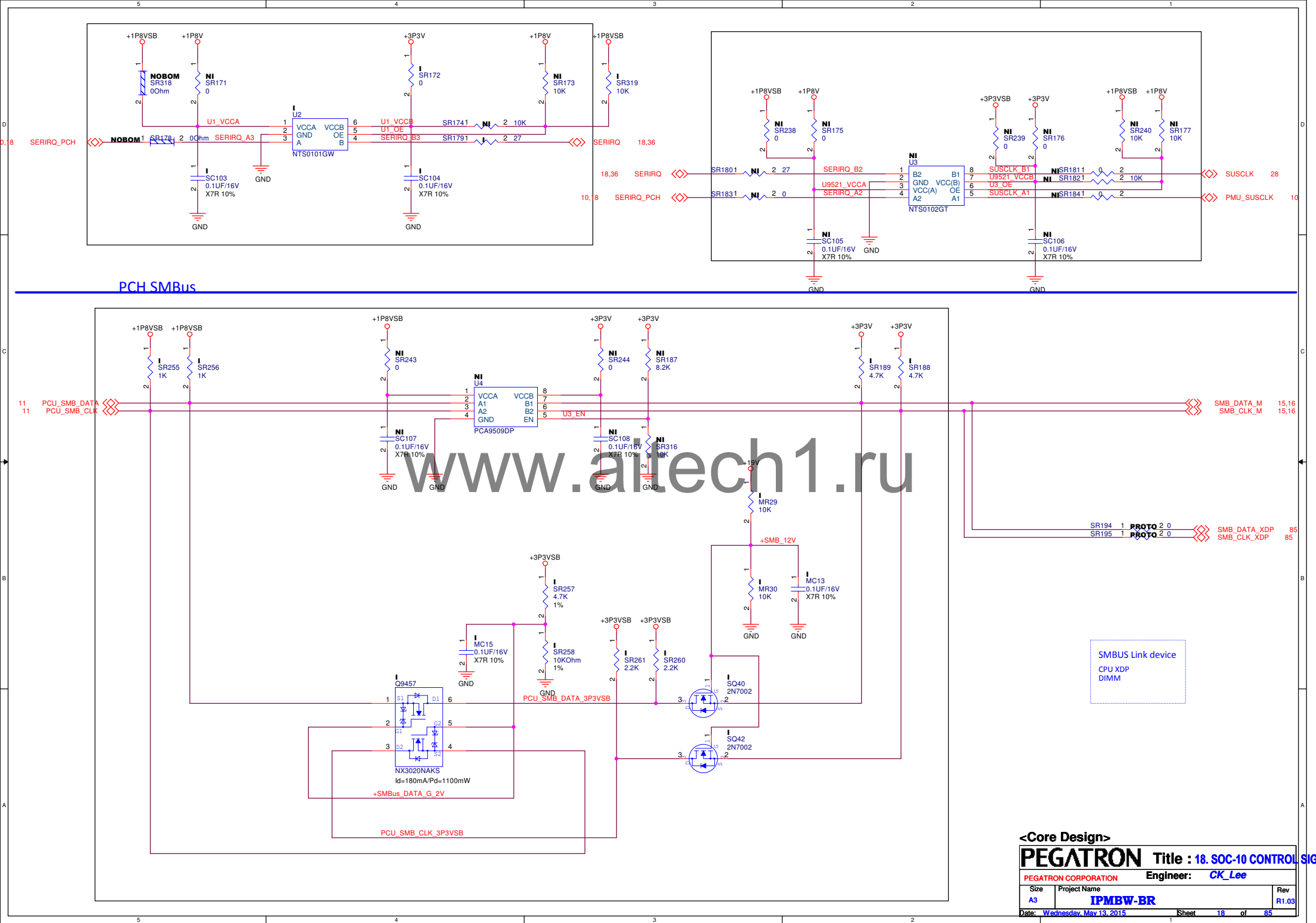
<Core Design>

PEGATRON Title : 17.DDR3 TERMINATION A&B

PEGATRON CORPORATION Engineer: CK_Lee

Size A3 Project Name IPMBW-BR Rev R1.03

Date: Wednesday, May 13, 2015 Sheet 17 of 85

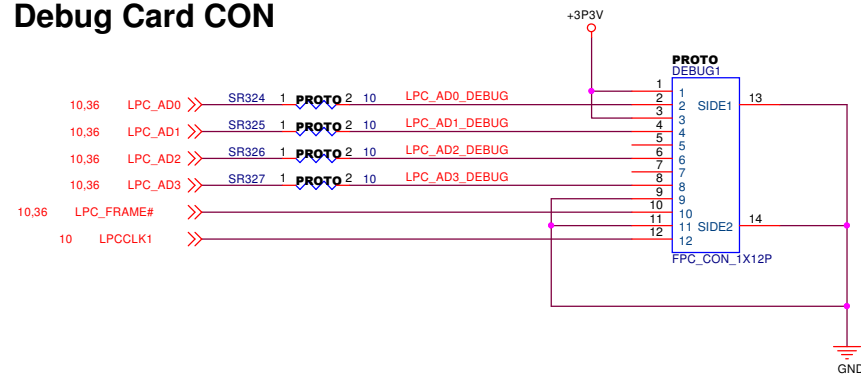


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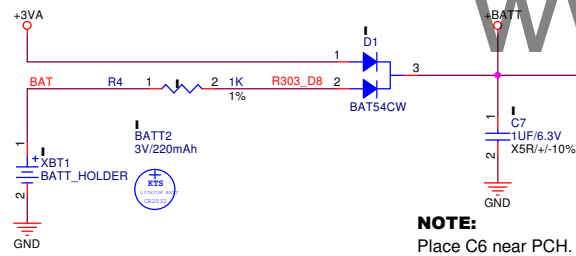
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PEGATRON		Title : 19. SOC-11 CONTROL SIGNAL	
PEGATRON CORPORATION		Engineer: CK_Lee	
Size	Project Name	Rev	
A3	IPMBW-BR	R1.03	
Date: Wednesday, May 13, 2015		Sheet 19 of 85	

Debug Card CON



External RTC Circuitry



CLR CMOS CIRCUIT



	CMOS RTC
1-2	DEFAULT
2-3	CLEAR

PEGATRON DT-MB RESTRICTED SECRET

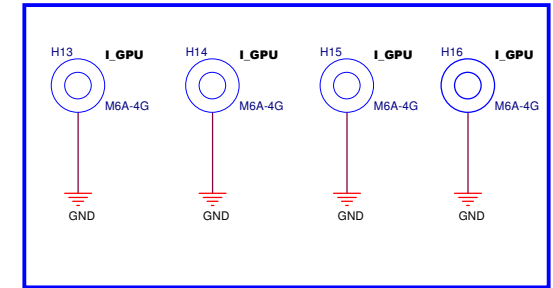
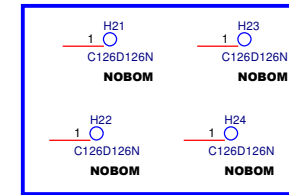
<Core Design>

PEGATRON		Title : 20.RTC/LPC DEBUG/CLR CMOS&PS	
PEGATRON CORPORATION		Engineer: CK_Lee	
Size A3	Project Name IPMBW-BR		Rev R1.03
Date: Wednesday, May 13, 2015		Sheet 20 of 85	

PWM FAN

NUTS for Thermal (CPU)

NUTS for Thermal (GPU)



improve +VCC layout

place near CPU

place under dimm

place near Fan-IN

place near CPU

place under dimm

To EC RESET

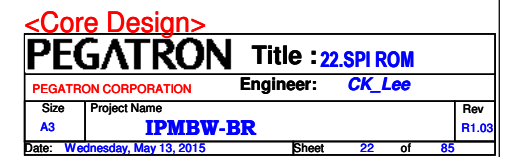
<Core Design>

PEGATRON Title : 21.FAN/HEATSINKTherm

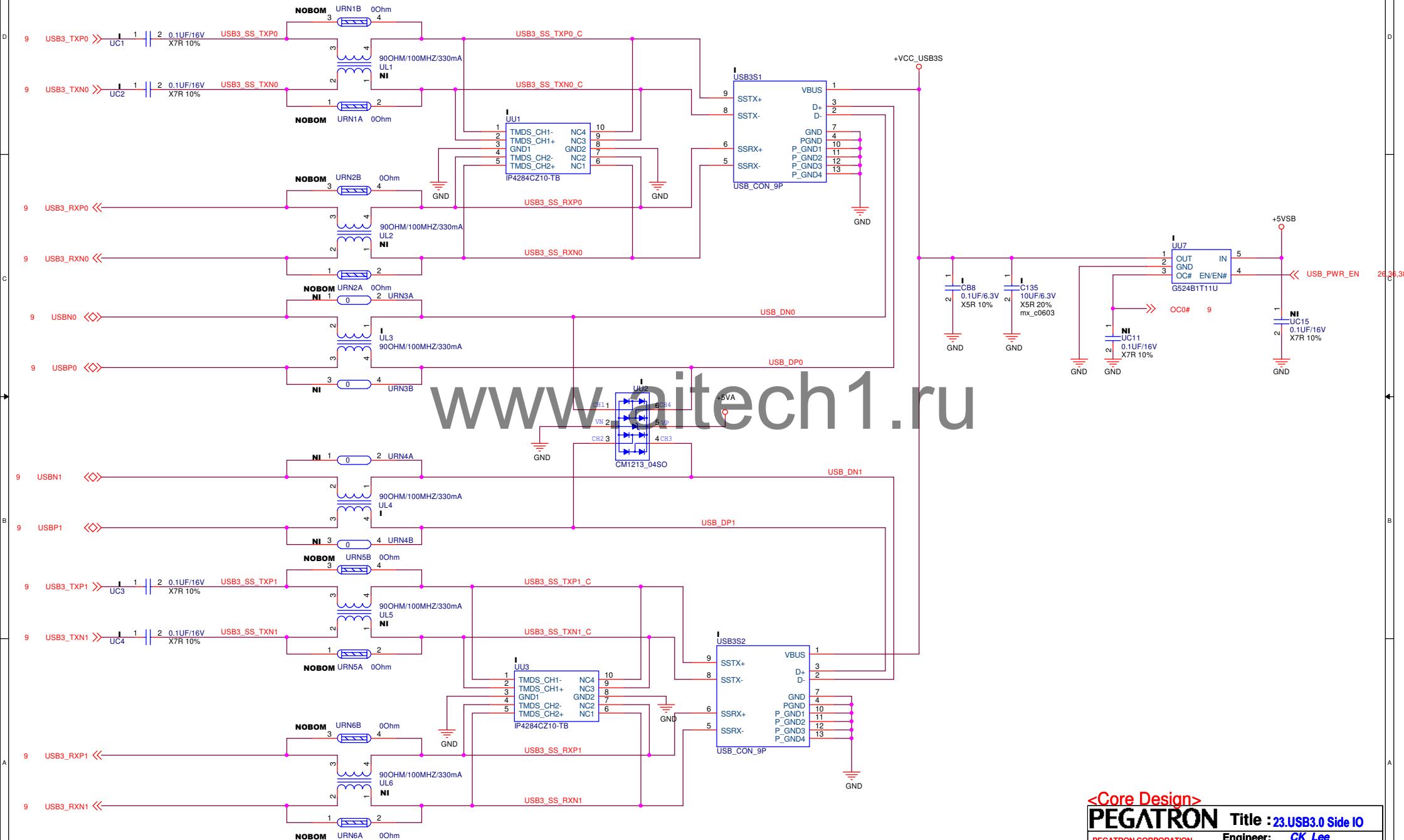
PEGATRON CORPORATION Engineer: CK_Lee

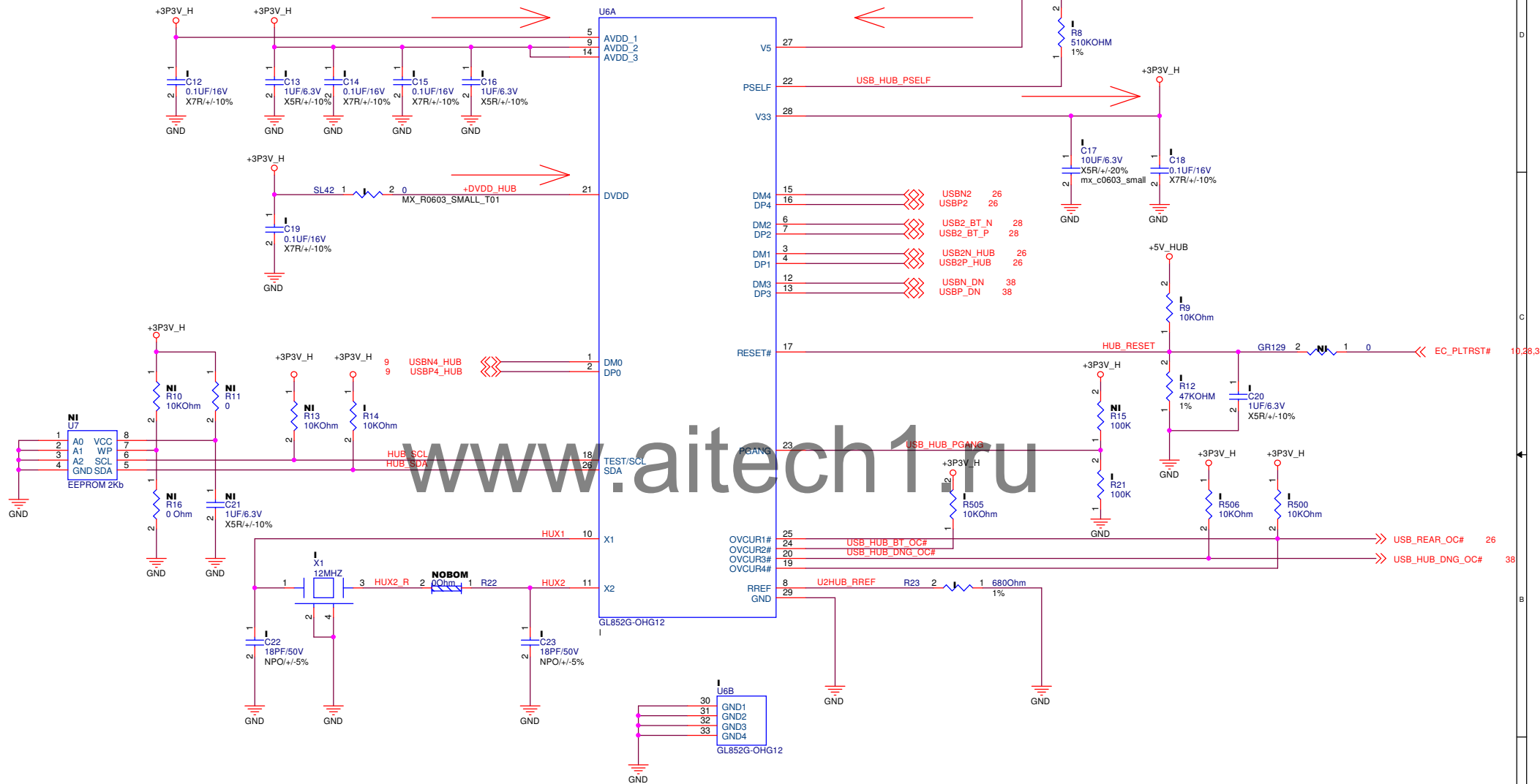
Size	Project Name	Rev
A3	IPMBW-BR	R1.03
Date: Wednesday, May 13, 2015	Sheet 21 of 85	

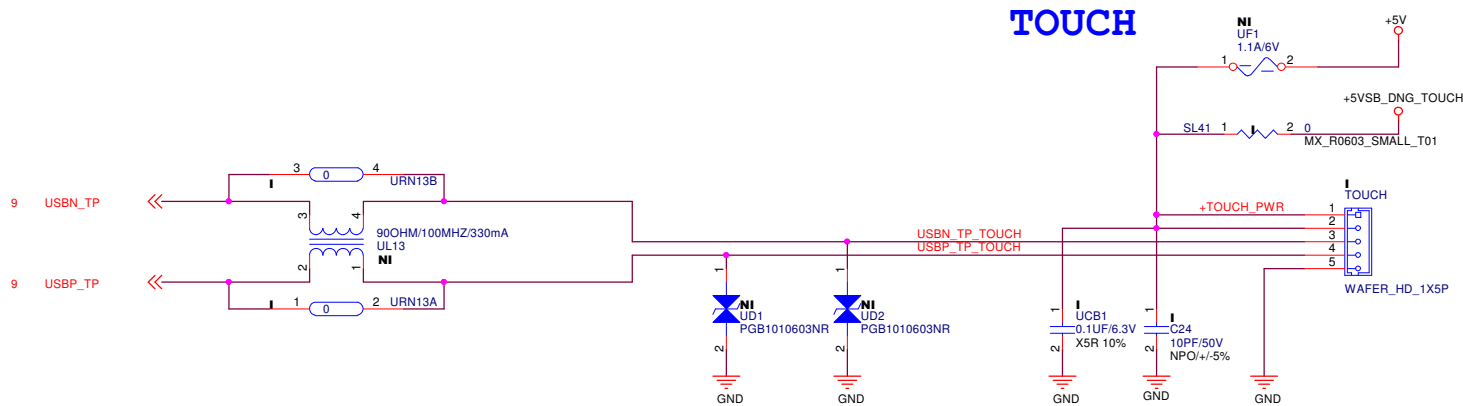
www.aitech1.ru



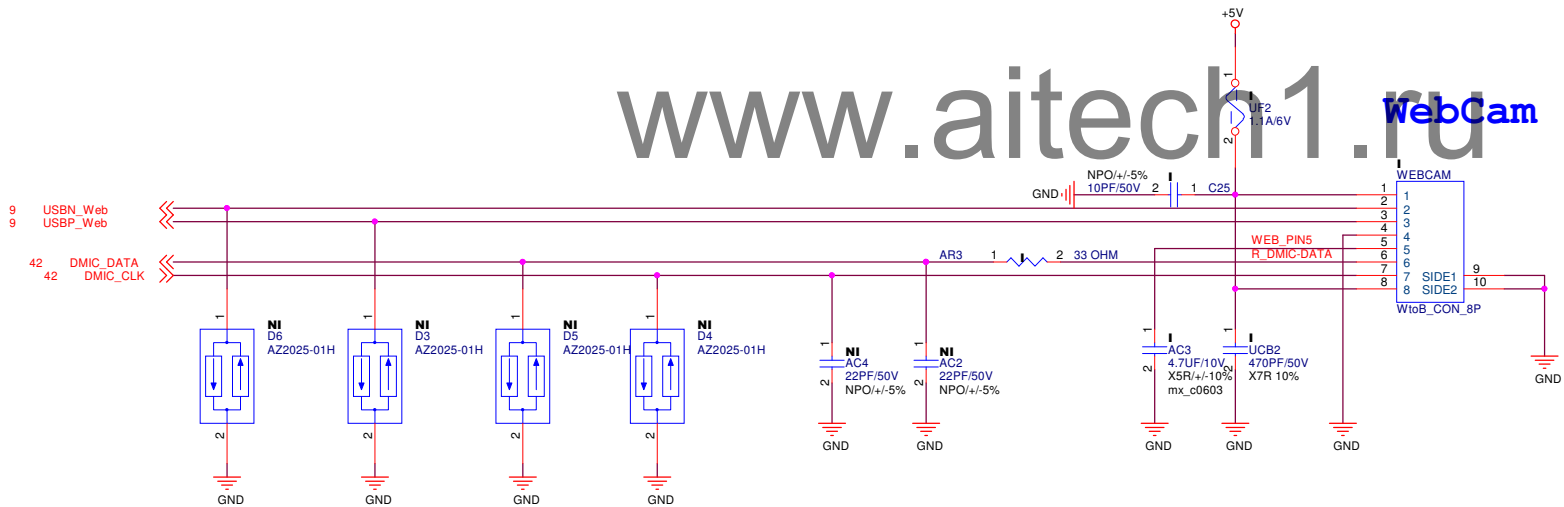
Side IO USB3.0







www.aitech1.ru WebCam



<Core Design>

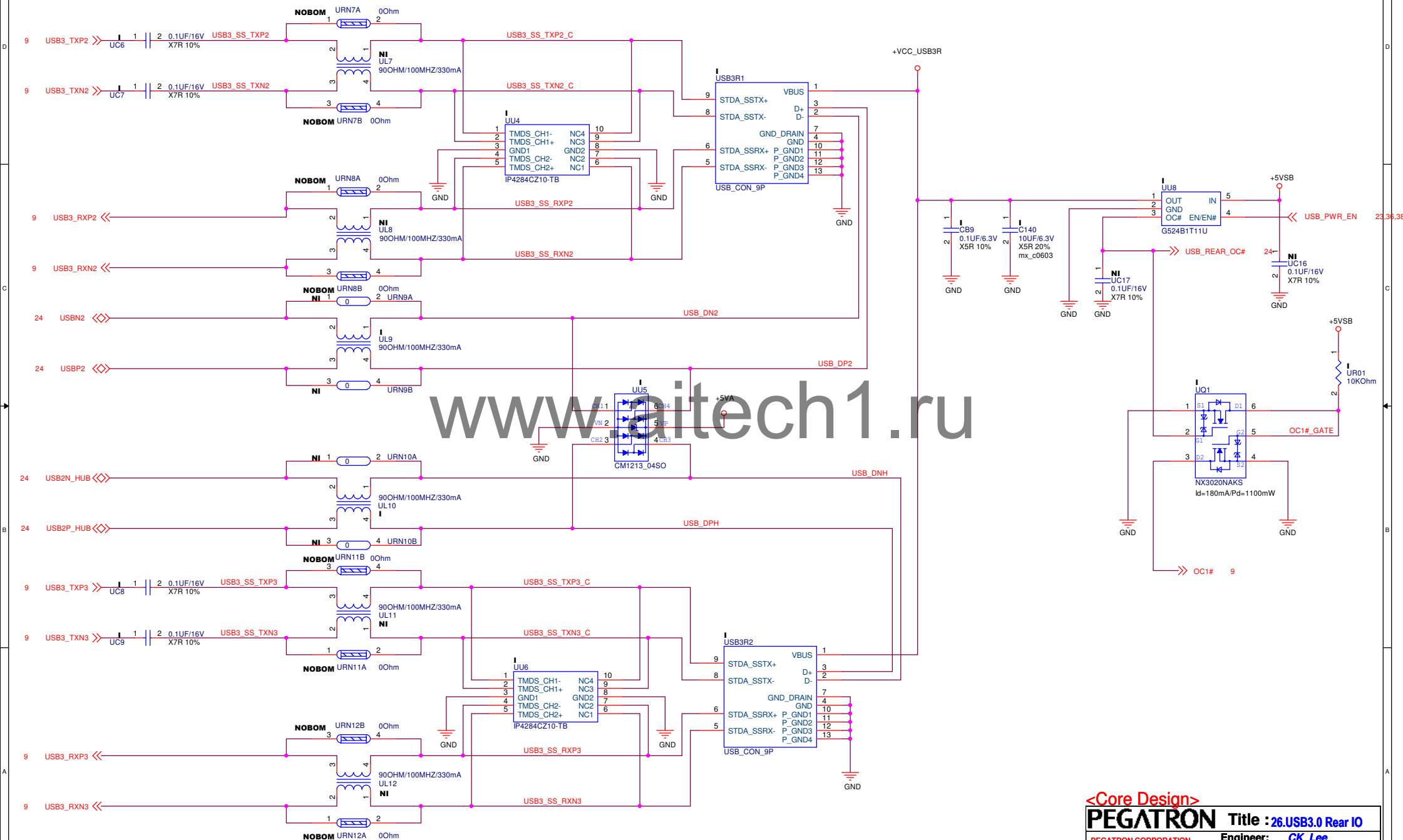
PEGATRON Title : 25.USB2.0 WebCam/Touch

PEGATRON CORPORATION Engineer: CK_Lee

Size A3 Project Name IPMBW-BR Rev R1.03

Date: Wednesday, May 13, 2015 Sheet 25 of 85

Rear IO USB3.0



<Core Design>

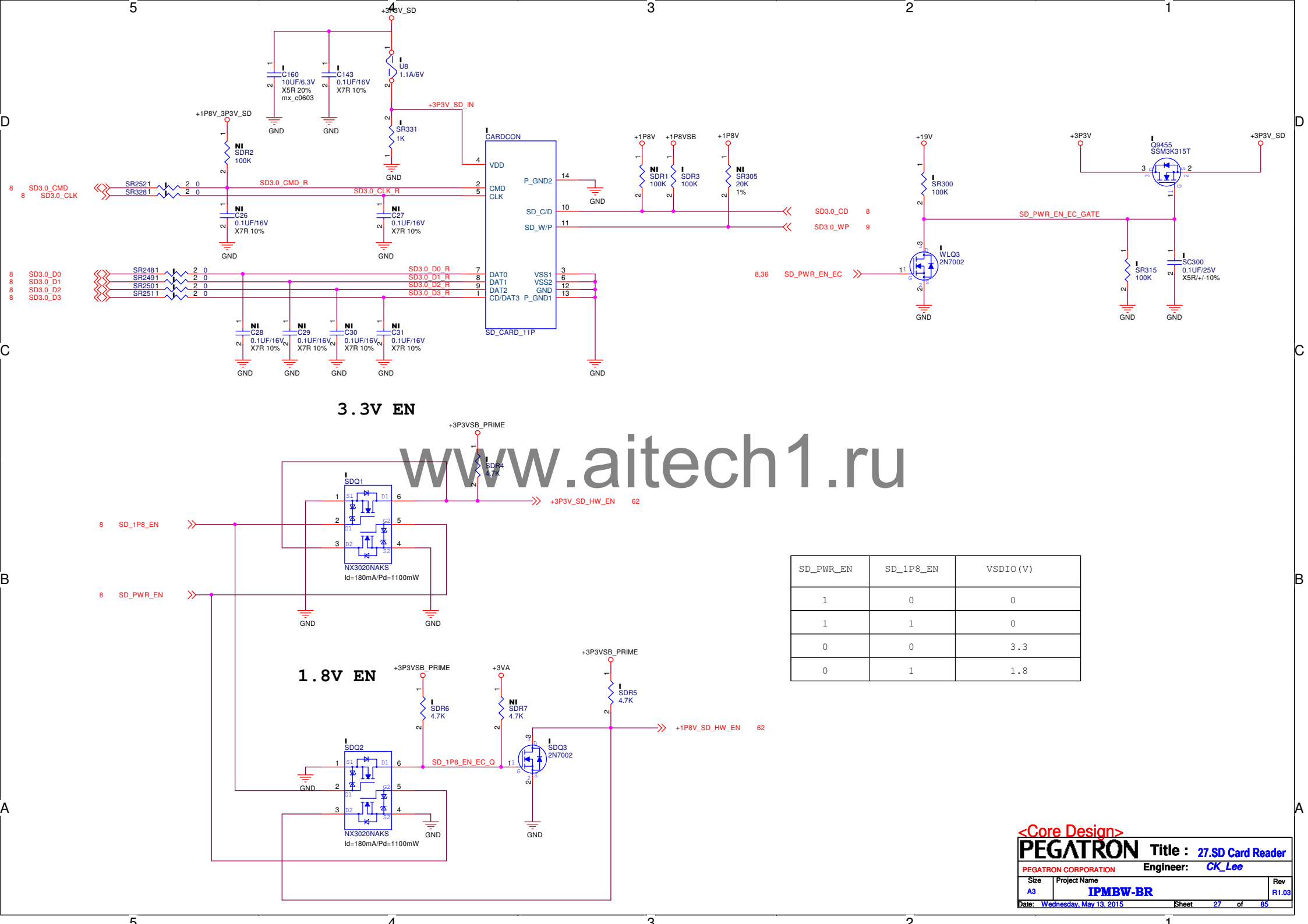
PEGATRON Title : 26.USB3.0 Rear IO

PEGATRON CORPORATION Engineer: CK_Lee

Size Project Name Rev

A3 IPMBW-BR R1.03

Date: Wednesday, May 13, 2015 Sheet 26 of 85

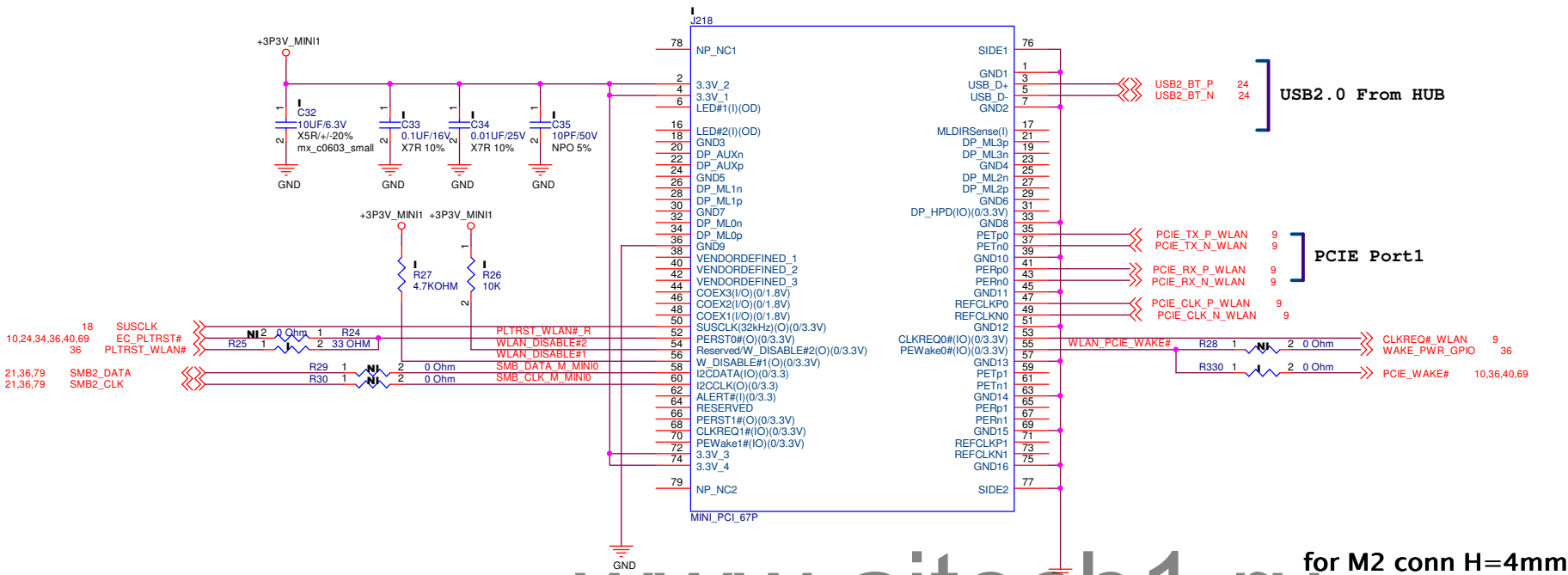


3.3V EN

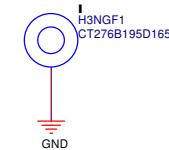
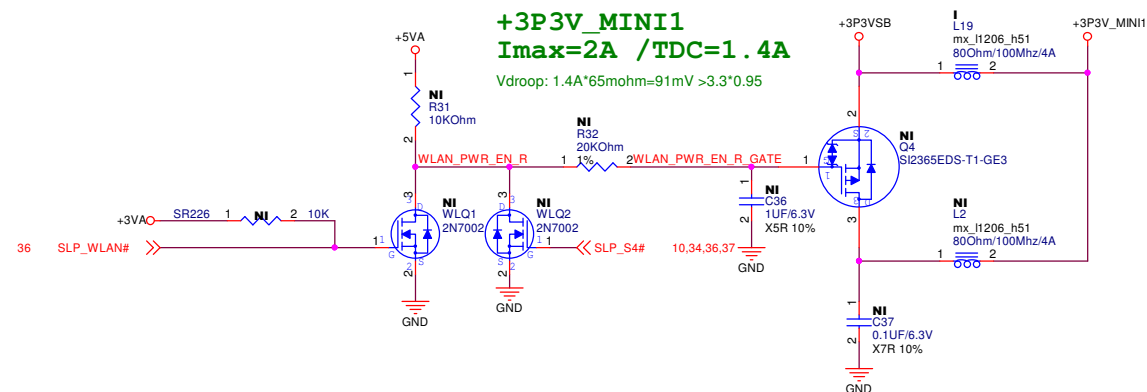
1.8V EN

SD_PWR_EN	SD_1P8_EN	VSDIO (V)
1	0	0
1	1	0
0	0	3.3
0	1	1.8

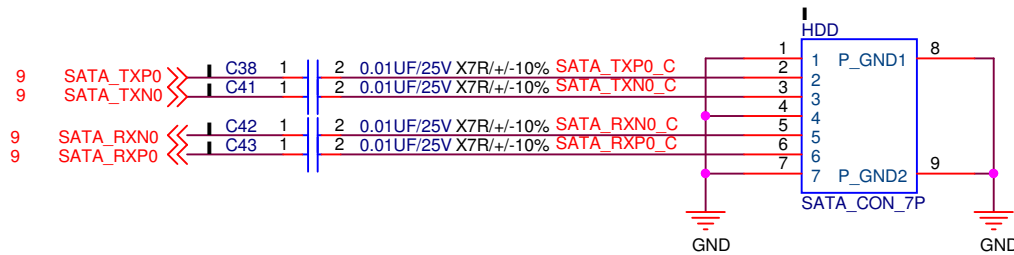
MiniCard for WiFi



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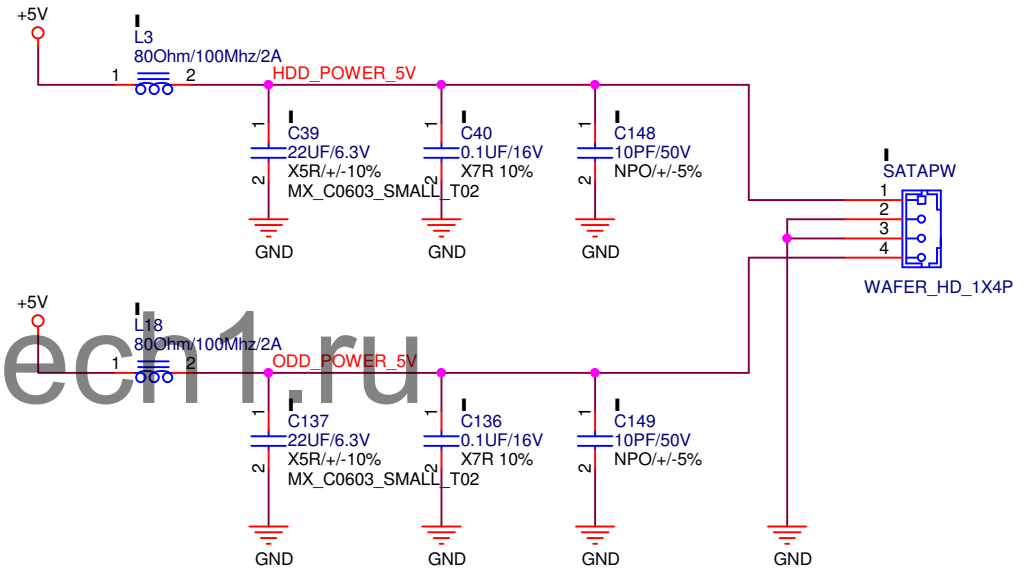
SATA HDD CON



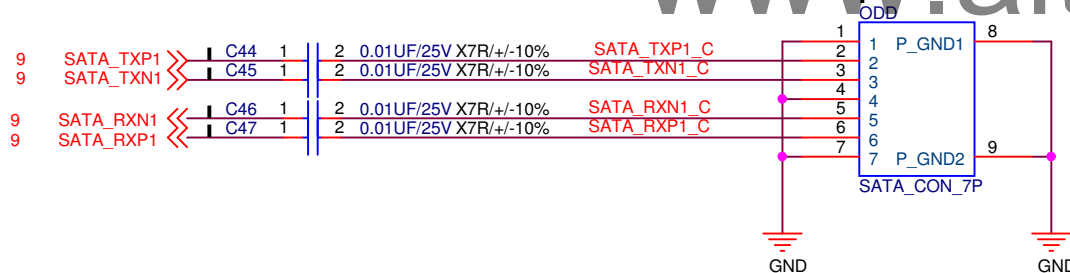
SATA CONTROLLER #1 (MASTER)

COLOR = DARK BLUE

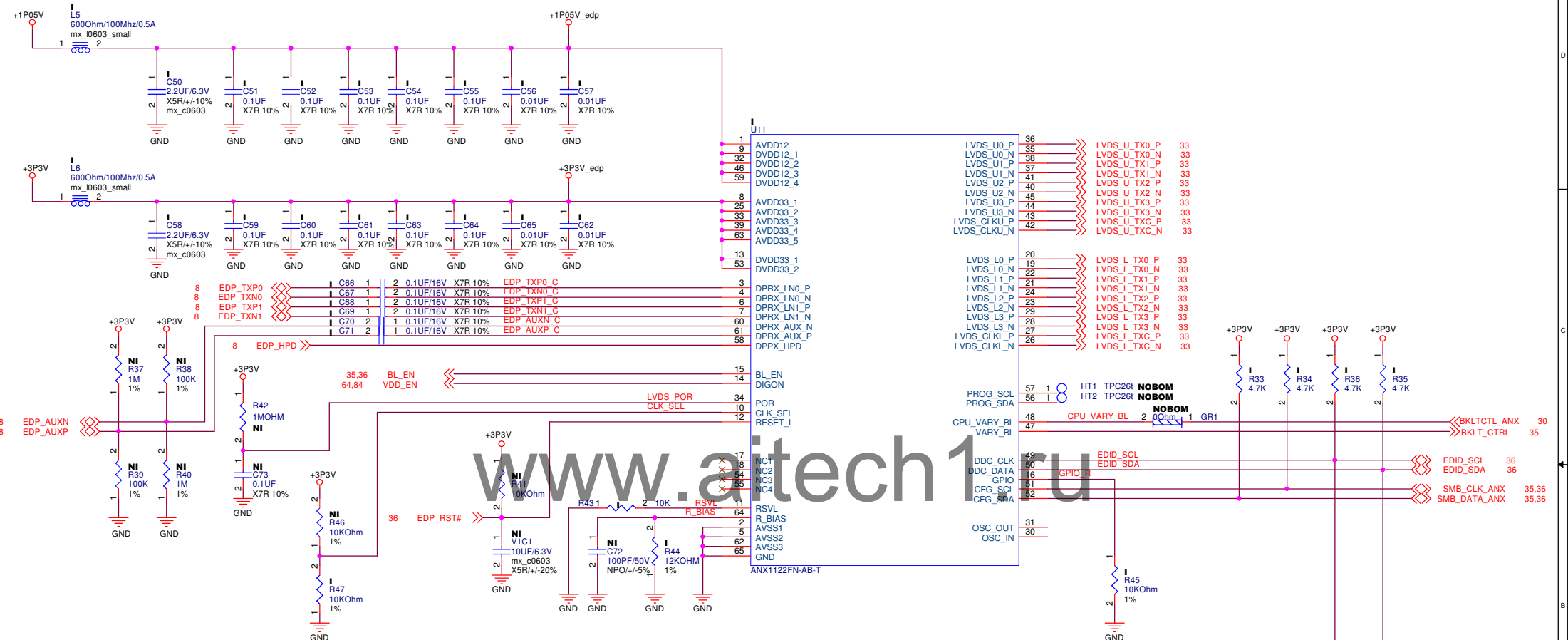
SATA POWER CONN FOR HDD/ODD



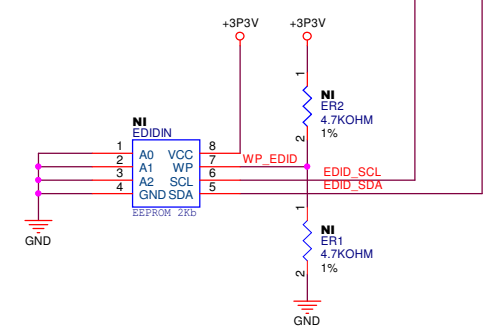
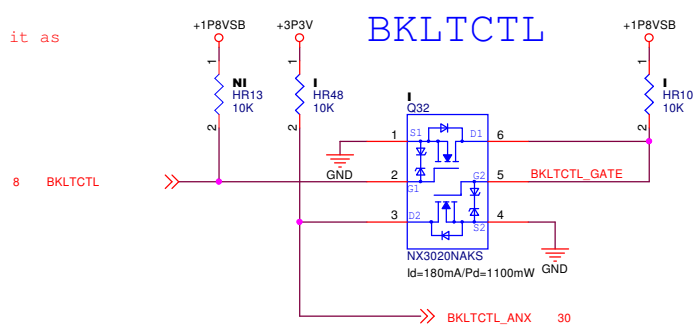
SATA ODD CON

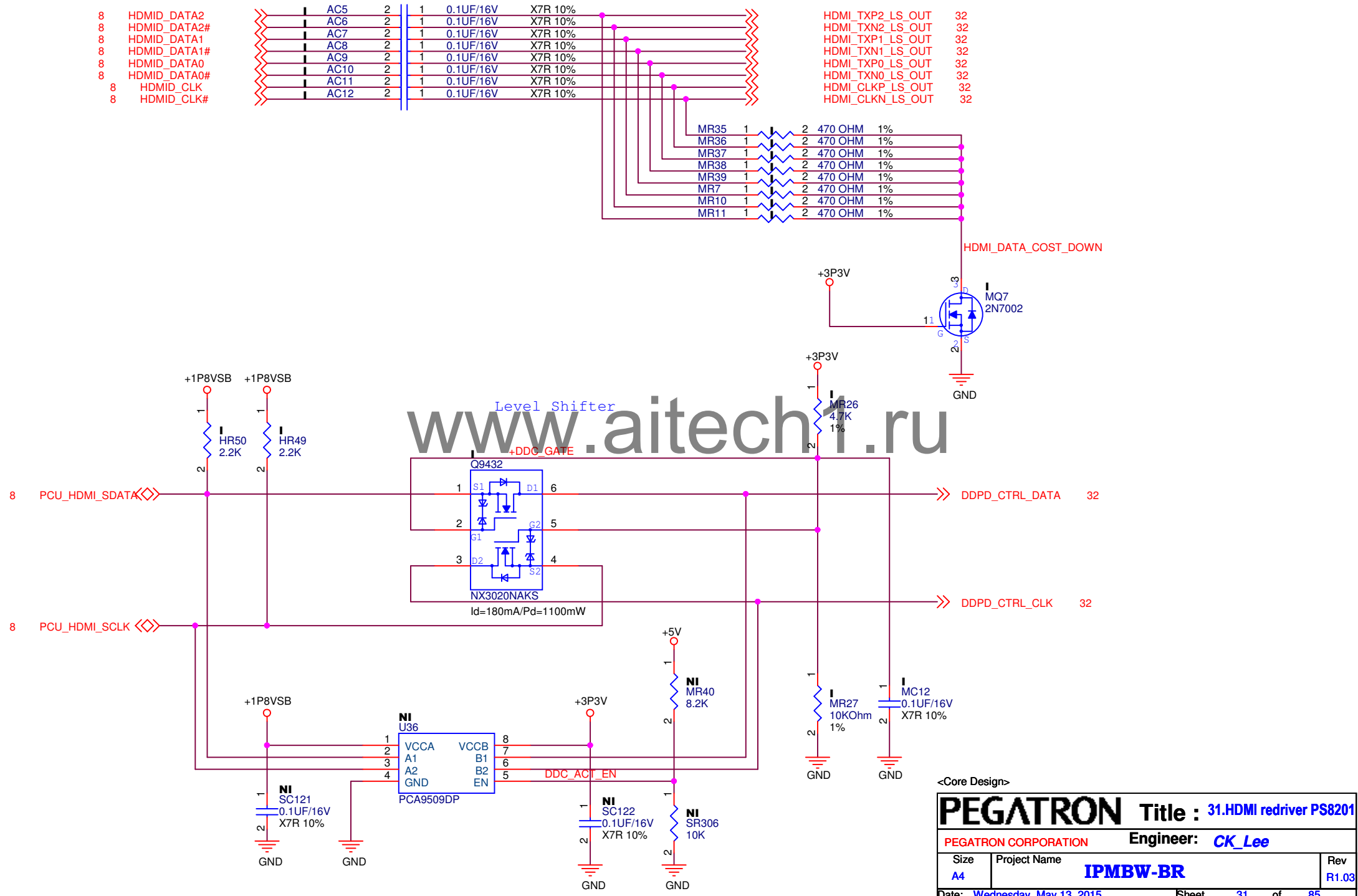


SATA CONTROLLER #2 (SLAVE)



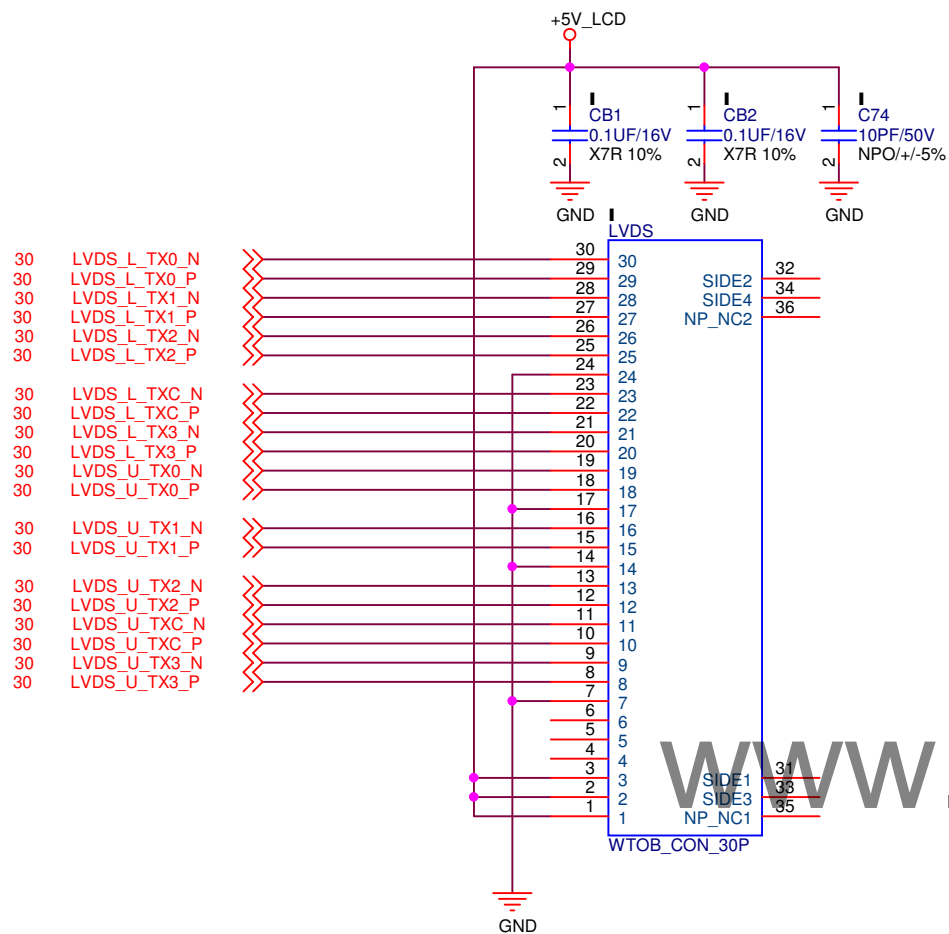
Input CLK selection
Pull up: work with 100M clock from Pin 30/31.
Pull down: work with on chip OSC and Pin 30/31 leave it as floating pin





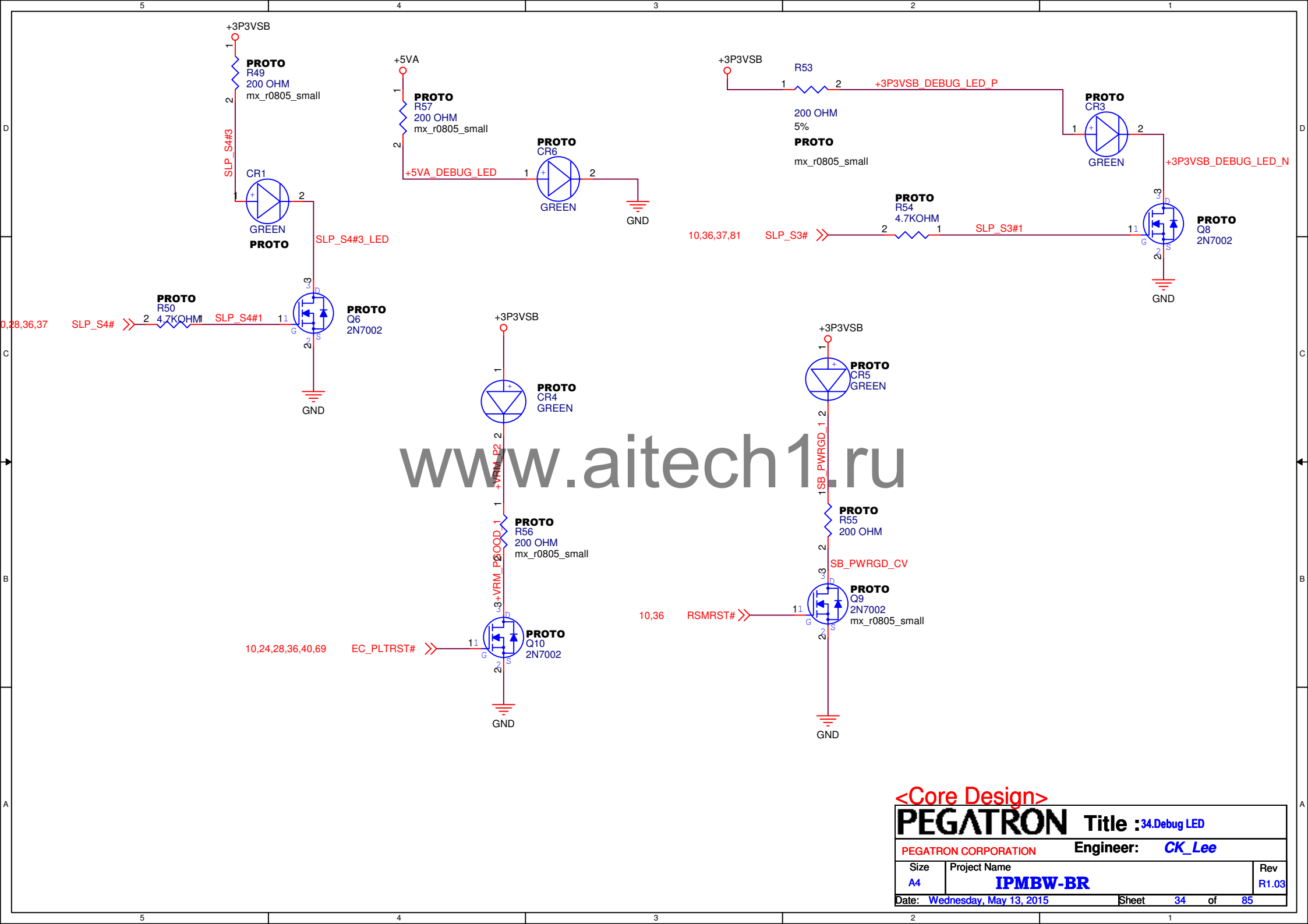
<Core Design>

PEGATRON		Title : 31.HDMI redriver PS8201	
PEGATRON CORPORATION		Engineer: CK_Lee	
Size A4	Project Name IPMBW-BR	Rev R1.03	
Date: Wednesday, May 13, 2015		Sheet	31 of 85



Pin	Name	Description
1	RXO0-	Negative LVDS differential data input. Channel O0 (odd)
2	RXO0+	Positive LVDS differential data input. Channel O0 (odd)
3	RXO1-	Negative LVDS differential data input. Channel O1 (odd)
4	RXO1+	Positive LVDS differential data input. Channel O1 (odd)
5	RXO2-	Negative LVDS differential data input. Channel O2 (odd)
6	RXO2+	Positive LVDS differential data input. Channel O2 (odd)
7	GND	Ground
8	RXOC-	Negative LVDS differential clock input. (odd)
9	RXOC+	Positive LVDS differential clock input. (odd)
10	RXO3-	Negative LVDS differential data input. Channel O3(odd)
11	RXO3+	Positive LVDS differential data input. Channel O3 (odd)
12	RXE0-	Negative LVDS differential data input. Channel E0 (even)
13	RXE0+	Positive LVDS differential data input. Channel E0 (even)
14	GND	Ground
15	RXE1-	Negative LVDS differential data input. Channel E1 (even)
16	RXE1+	Positive LVDS differential data input. Channel E1 (even)
17	GND	Ground
18	RXE2-	Negative LVDS differential data input. Channel E2 (even)
19	RXE2+	Positive LVDS differential data input. Channel E2 (even)
20	RXEC-	Negative LVDS differential clock input. (even)
21	RXEC+	Positive LVDS differential clock input. (even)
22	RXE3-	Negative LVDS differential data input. Channel E3 (even)
23	RXE3+	Positive LVDS differential data input. Channel E3 (even)

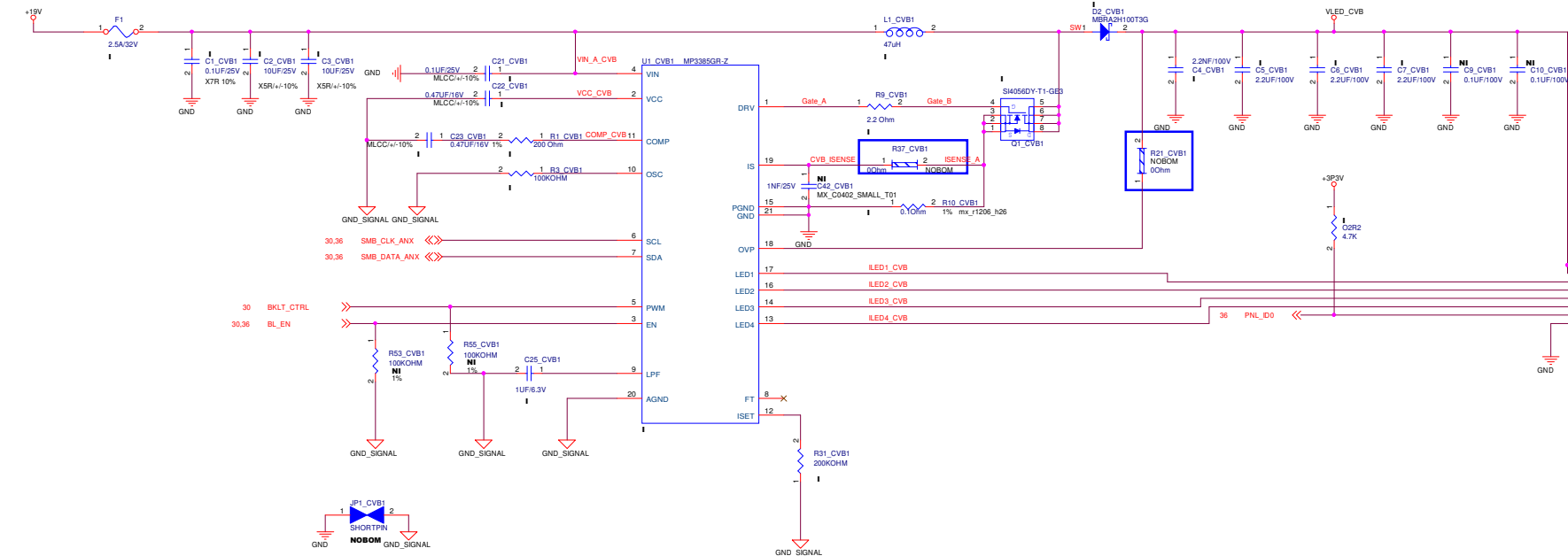
24	GND	Ground
25	NC	For LCD internal use only, Do not connect
26	NC	For LCD internal use only, Do not connect
27	NC	For LCD internal use only, Do not connect
28	Vcc	+5.0V power supply
29	Vcc	+5.0V power supply
30	Vcc	+5.0V power supply



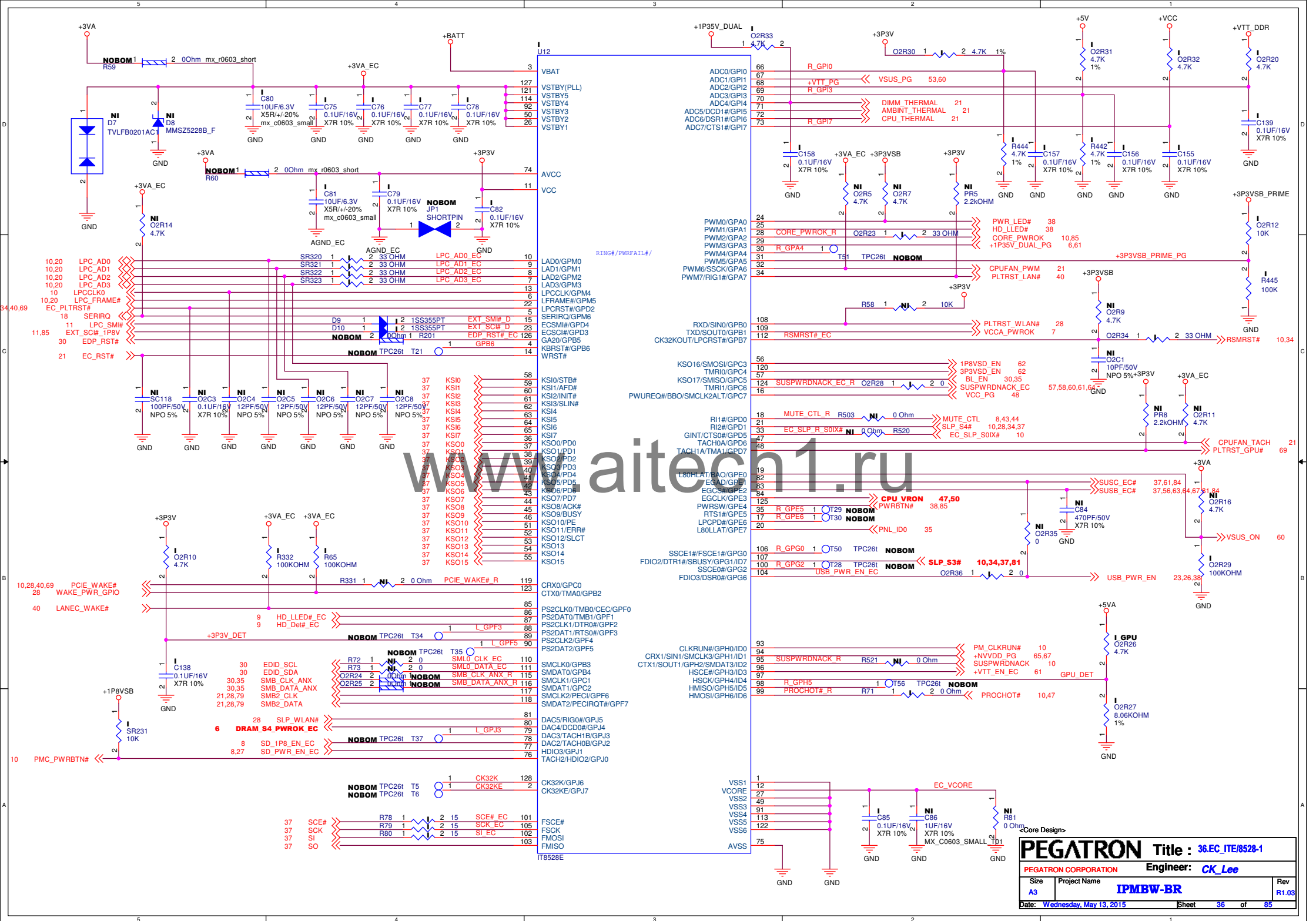
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PEGATRON		Title :34.Debug LED	
PEGATRON CORPORATION		Engineer: CK_Lee	
Size	Project Name		Rev
A4	IPMBW-BR		R1.03
Date: Wednesday, May 13, 2015		Sheet	34 of 85

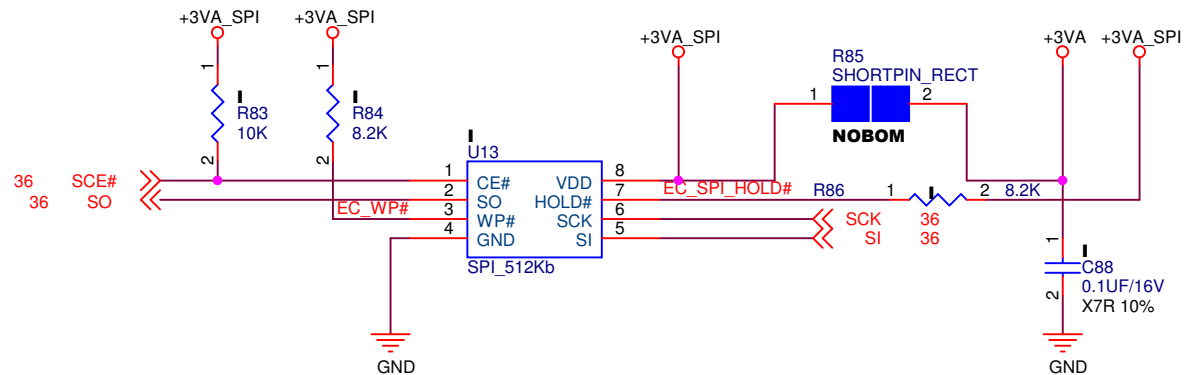
www.aitech1.ru



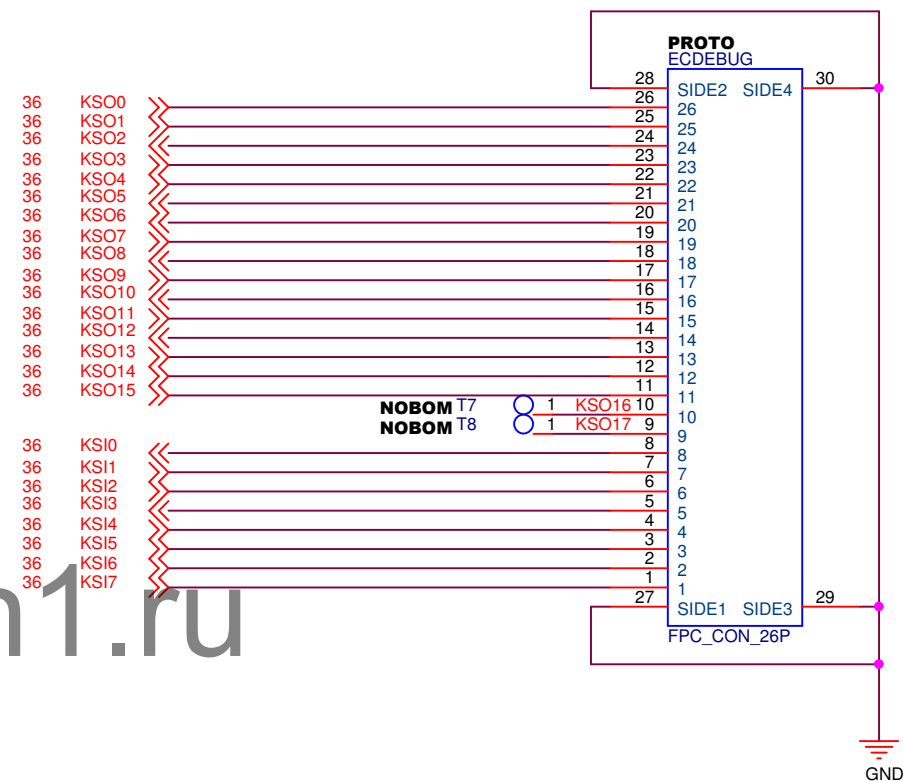
BL_EN	NOROM1	TPC26T
SMB_CLK_ANX	NOROM1	TPC26T
SMB_DATA_ANX	NOROM1	TPC26T
BKLT_CTRL	NOROM1	TPC26T
GND	NOROM1	TPC26T
VLED_CVB	NOROM1	TPC26T
ILED1_CVB	NOROM1	TPC26T
ILED2_CVB	NOROM1	TPC26T
ILED3_CVB	NOROM1	TPC26T
ILED4_CVB	NOROM1	TPC26T
PNL_ID0	NOROM1	TPC26T
GND	NOROM1	TPC26T
GND	NOROM1	TPC26T
GND	NOROM1	TPC26T
GND	NOROM1	TPC26T
GND	NOROM1	TPC26T



SPI ROM+ External programming conn.



Keyboard Connector(debug)



For EC PU/PD



<Core Design>

PEGATRON Title : 37.EC ITE/8528-2

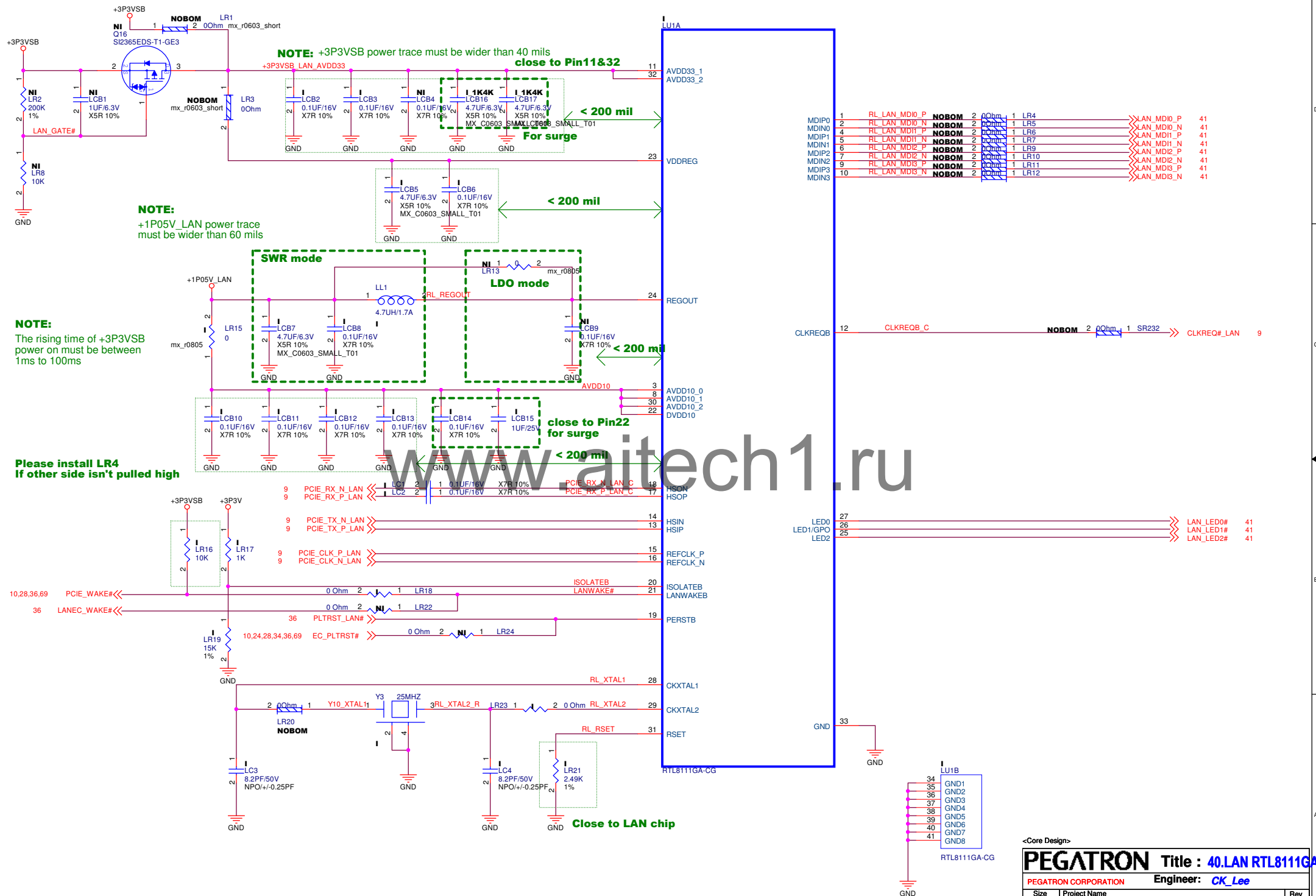
PEGATRON CORPORATION Engineer: **CK Lee**

Size A4	Project Name IPMBW-BR	Rev R1.03
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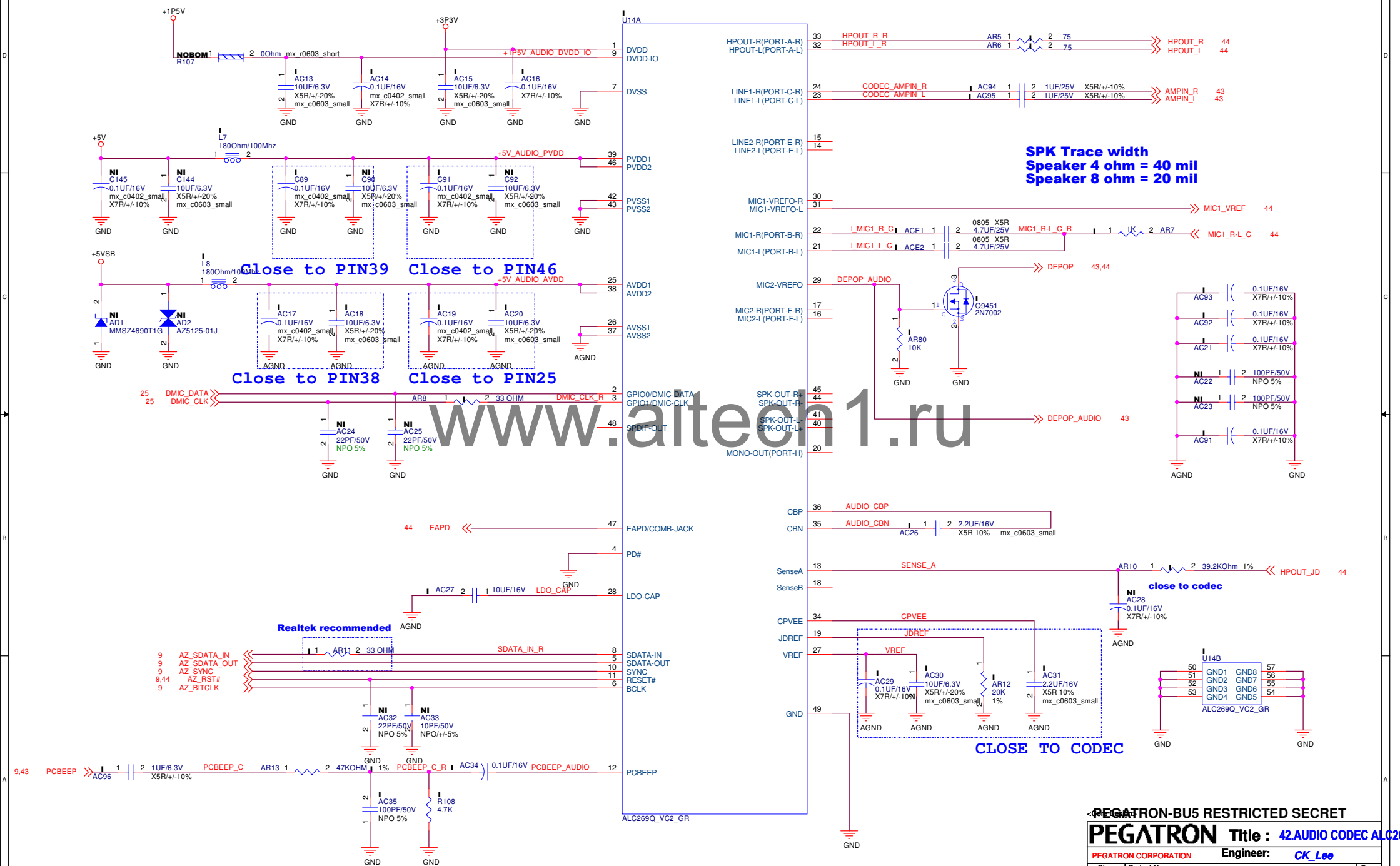
Date: **Wednesday, May 13, 2015** Sheet **37** of **85**

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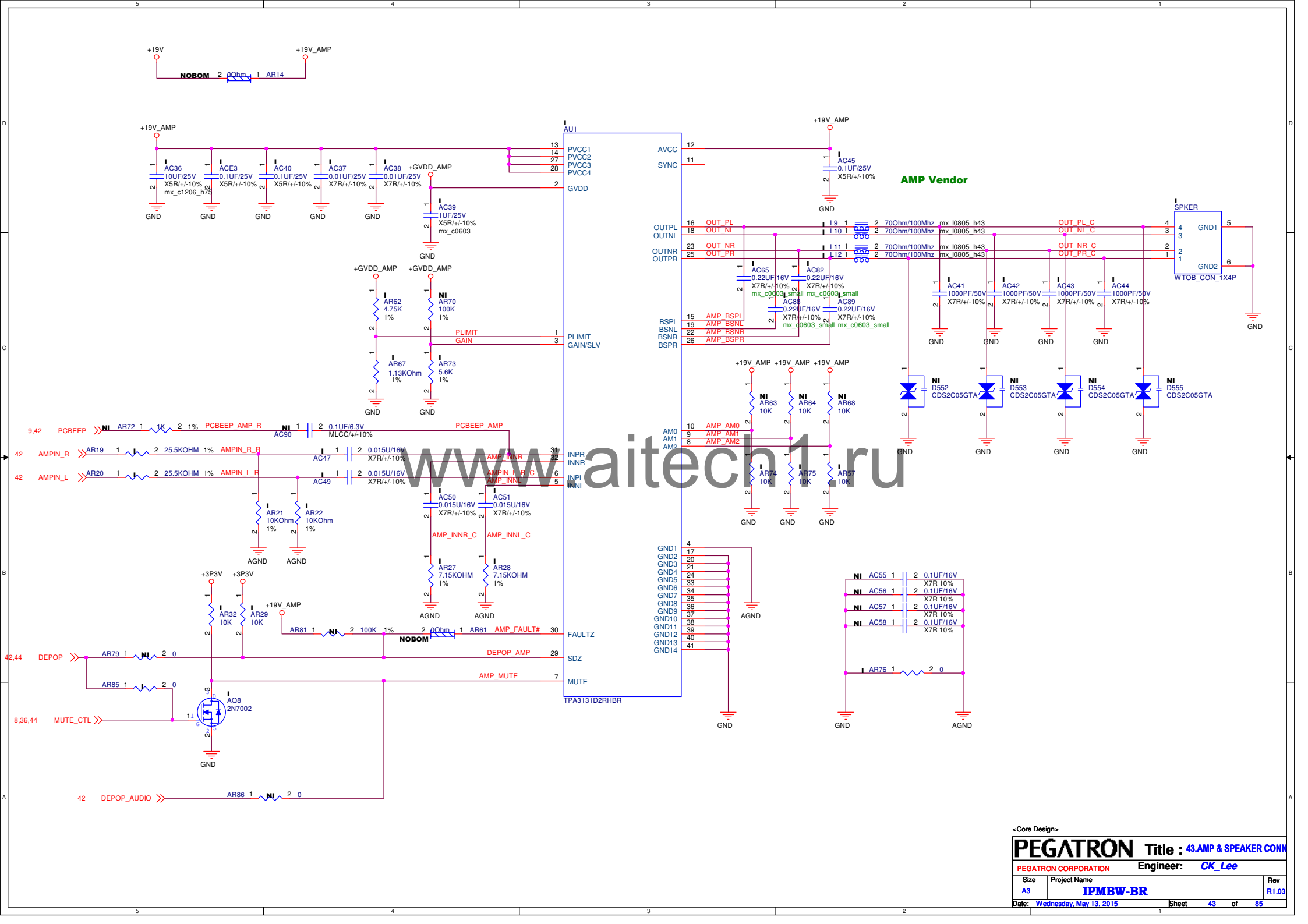
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PEGATRON		Title : 39.xxxxxxx
PEGATRON CORPORATION		Engineer: CK_Lee
Size A4	Project Name IPMBW-BR	Rev R1.03
Date: Wednesday, May 13, 2015		Sheet 39 of 85



ALC269 CODEC



<PEGATRON-BU5 RESTRICTED SECRET			
PEGATRON		Title : 42.AUDIO CODEC AL C2	
PEGATRON CORPORATION		Engineer: CK_Lee	
Size A3	Project Name IPMBW-BR	Rev R1.03	
Date: Wednesday, May 13, 2015		Sheet 42	of 85



<Core Design>

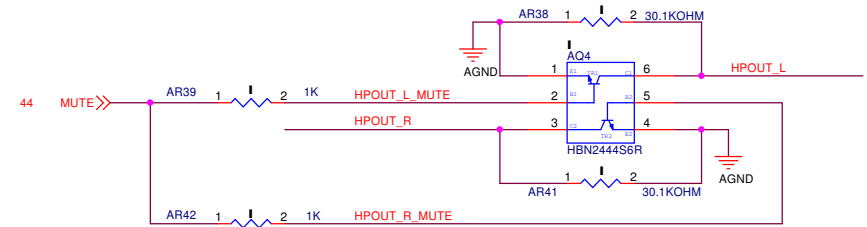
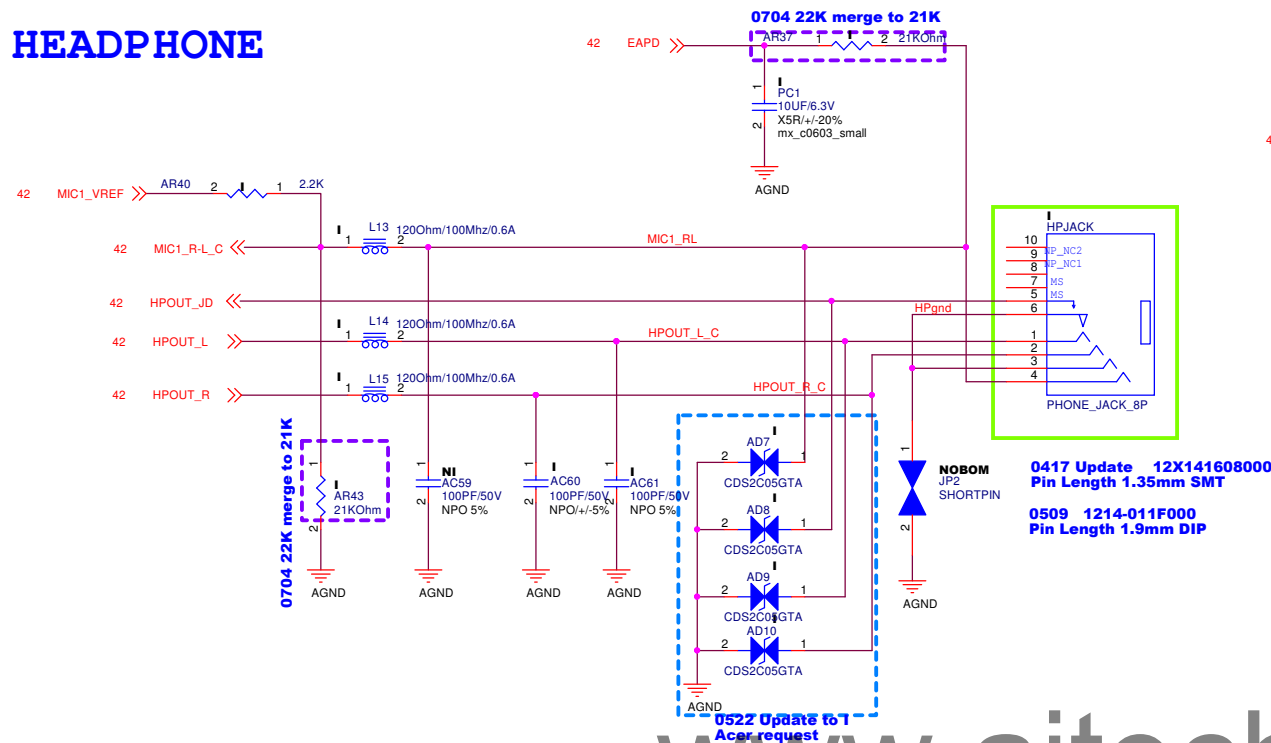
PEGATRON Title : 43.AMP & SPEAKER CONN

PEGATRON CORPORATION Engineer: CK_Lee

Size A3 Project Name IPMBW-BR Rev R1.03

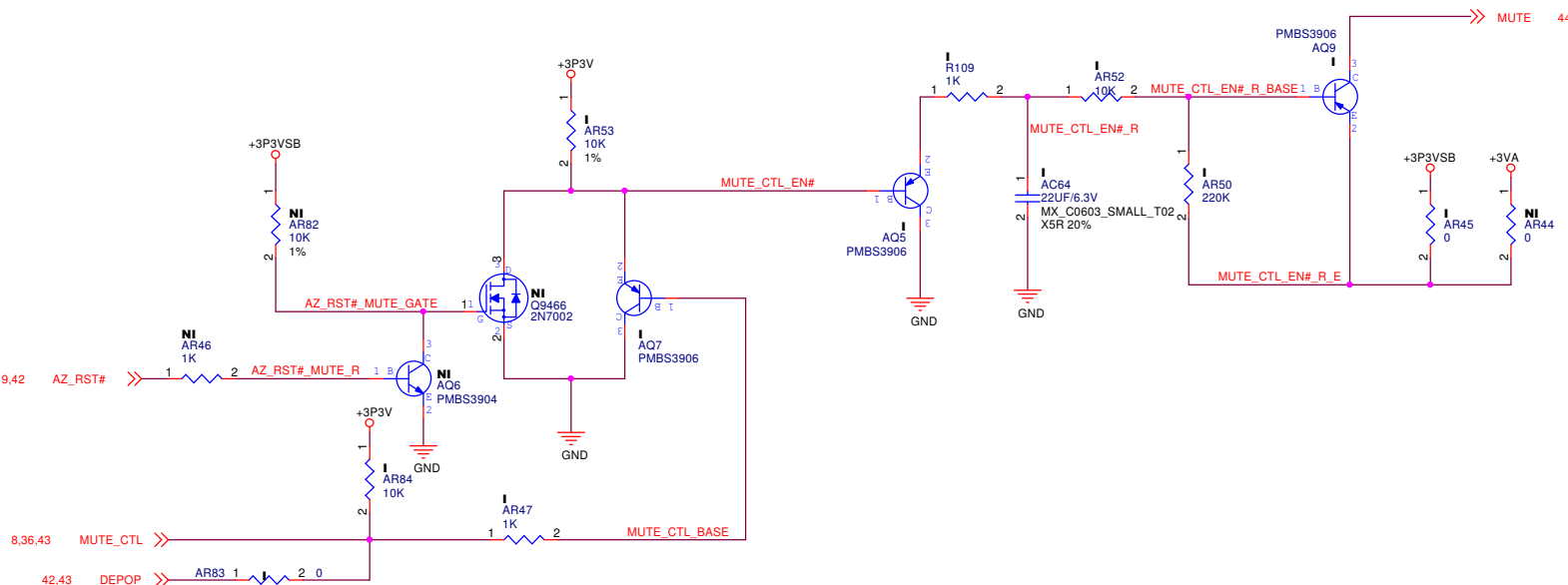
Date: Wednesday, May 13, 2015 Sheet 43 of 85

HEADPHONE



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Audio MUTE



PCB1
PCB BOARD

IPMBW-BR
PCB
Proprietary

SN_LABEL
42X7_WHITE

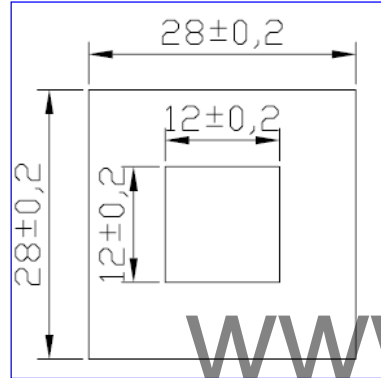
PPIDLB
PPID label

AMP
AMILB
AMI label

BPLATE
BACK PLATE

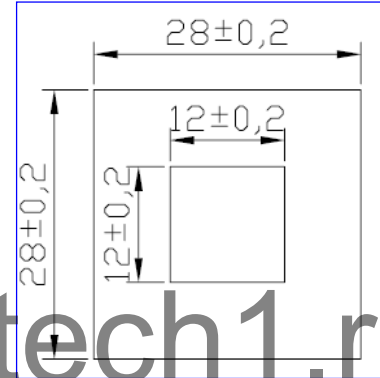
IPMBW-BR
BACK PLATE

MYLAR1



J1008607

GPU
MYLAR2



J1008607

www.aitech1.ru

<Core Design>

PEGATRON

Title : 45. PCB & Label & Mylar

PEGATRON CORPORATION

Engineer: CK_Lee

Size
A3

Project Name

IPMBW-BR

Rev

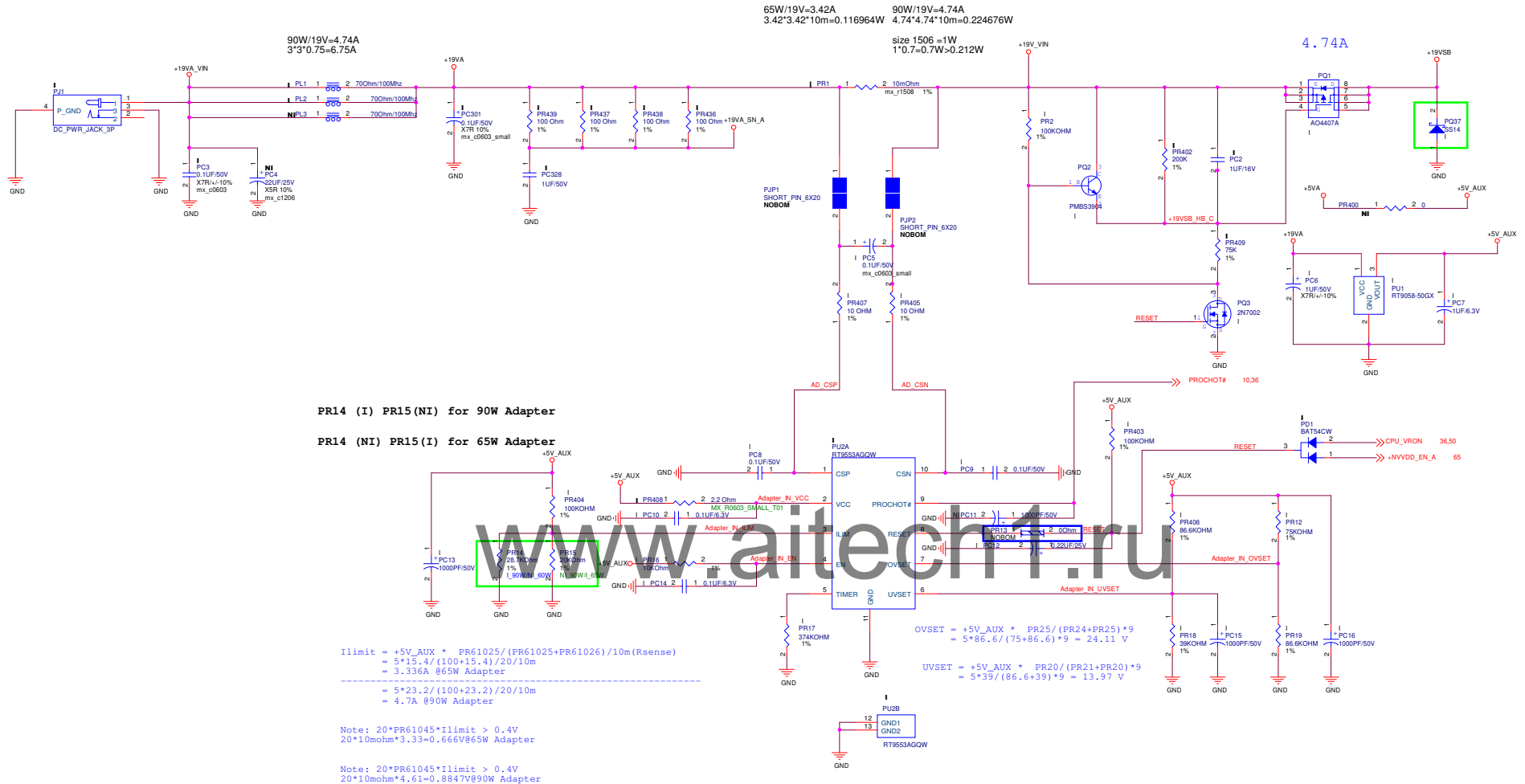
R1.03

Date: Wednesday, May 13, 2015

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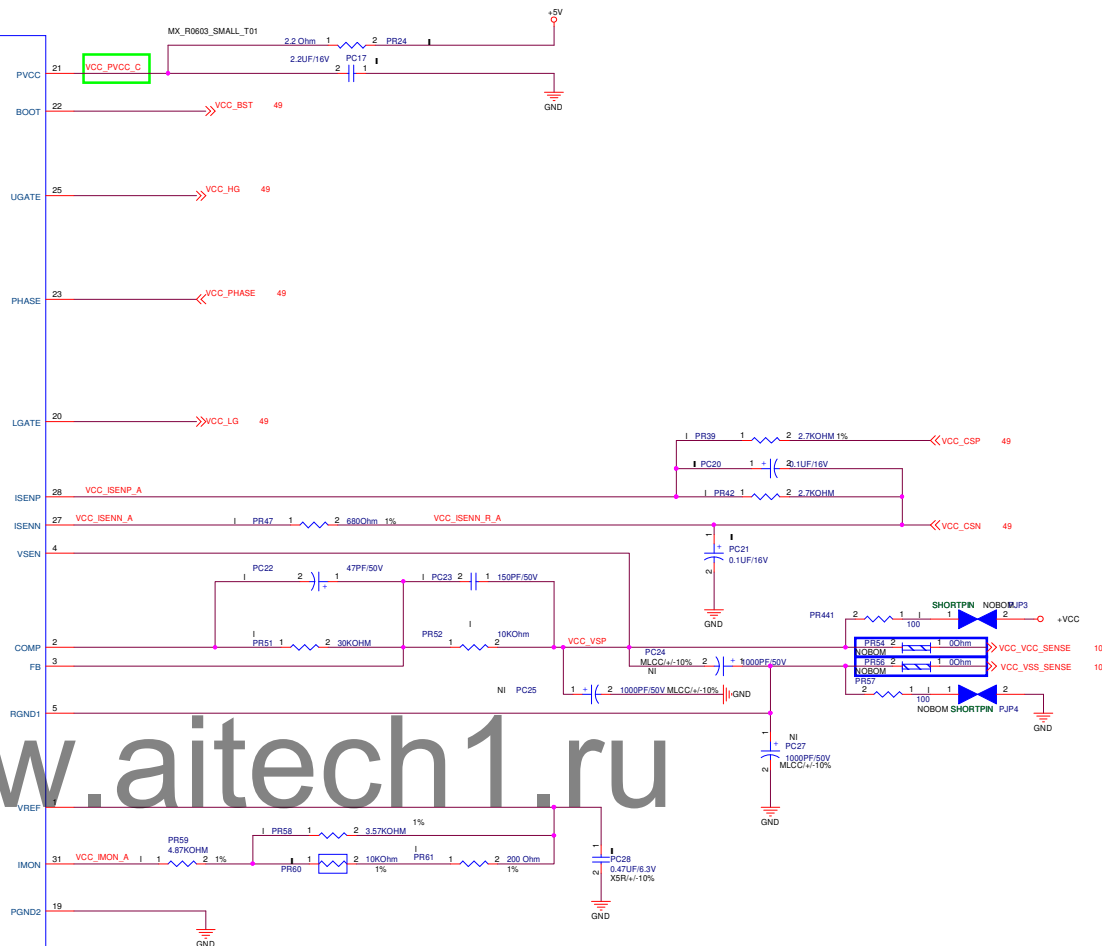
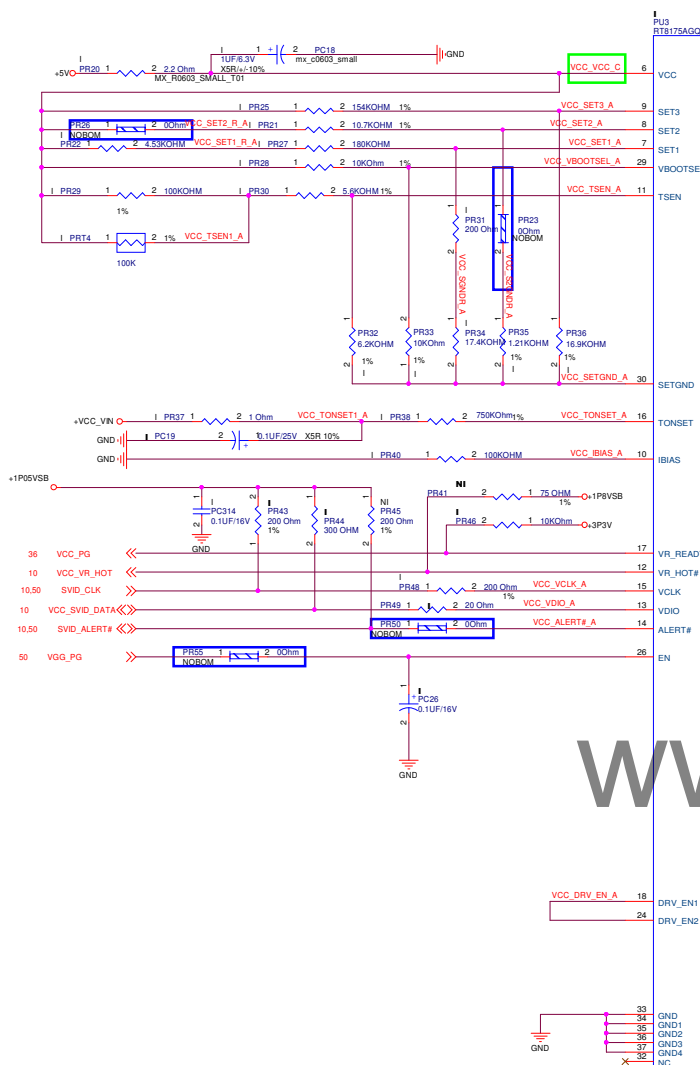
www.aitech1.ru

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PEGATRON		Title : 56. XXXXXX
PEGATRON CORPORATION		Engineer: CK_Lee
Size A3	Project Name IPMBW-BR	Rev R1.03
Date: Wednesday, May 13, 2015		Sheet 46 of 85



<Core Design>

File	<Title>	Rev
Size	Document Number	Rev
AC	PR40W-SR	P1.0
Date:	Wednesday, May 13, 2015	Sheet 47 of 85



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Size	Document Number	Rev	
A2	IPMBW-BR	R1.00	
Date	Wednesday, May 13, 2015	Sheet	48 of 85

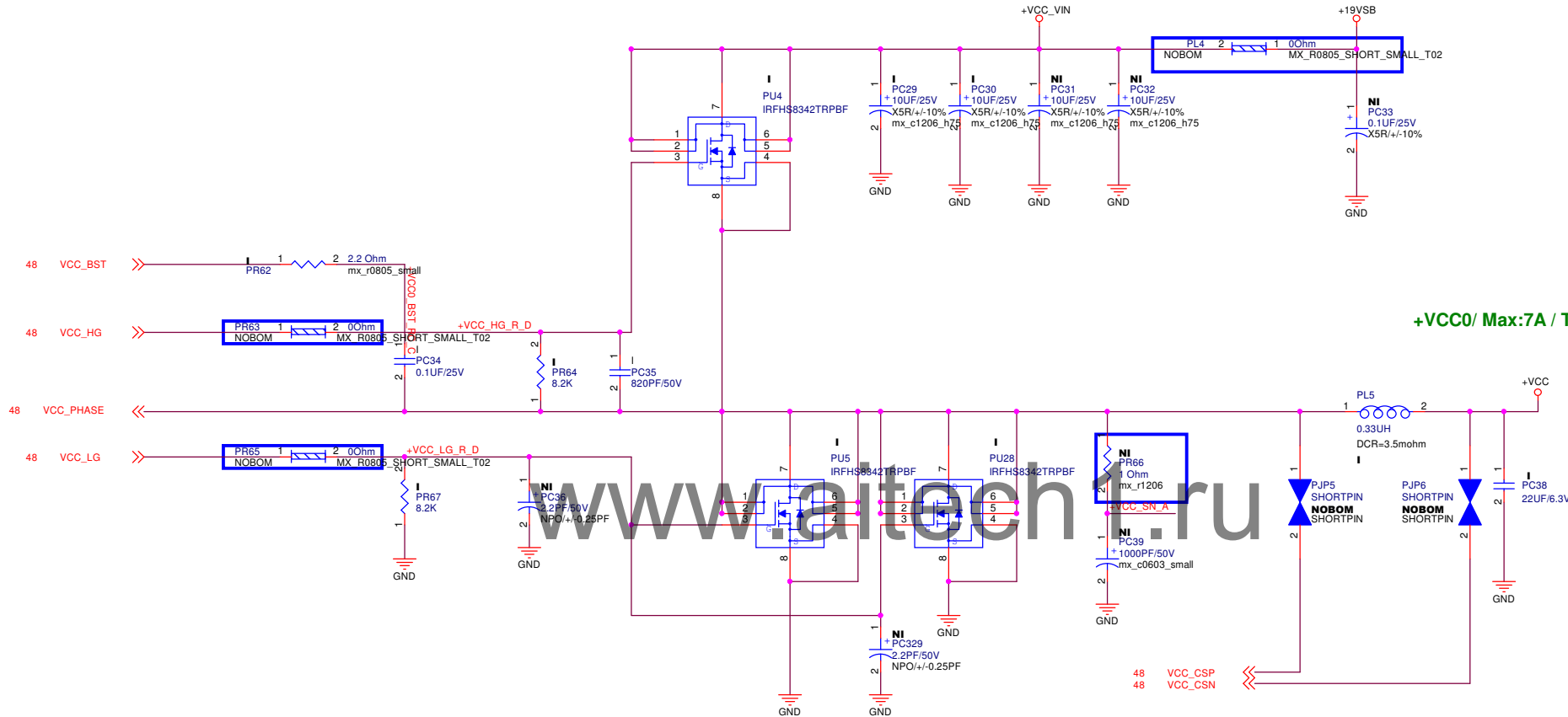
+VCC, PLACE NEAR CPU

$I_{in}=0.53A$

Fsw=500kHz
 $I_{in,rms}=0.29934$
 $I_{ripple}=2.37A$
 $L/S=0.227W$
 $L/S=0.793W$
 $OCP=14.5$

EFF=57.97%@10%Imax
 EFF=81.38%@TDC
 EFF=79.99%@Imax

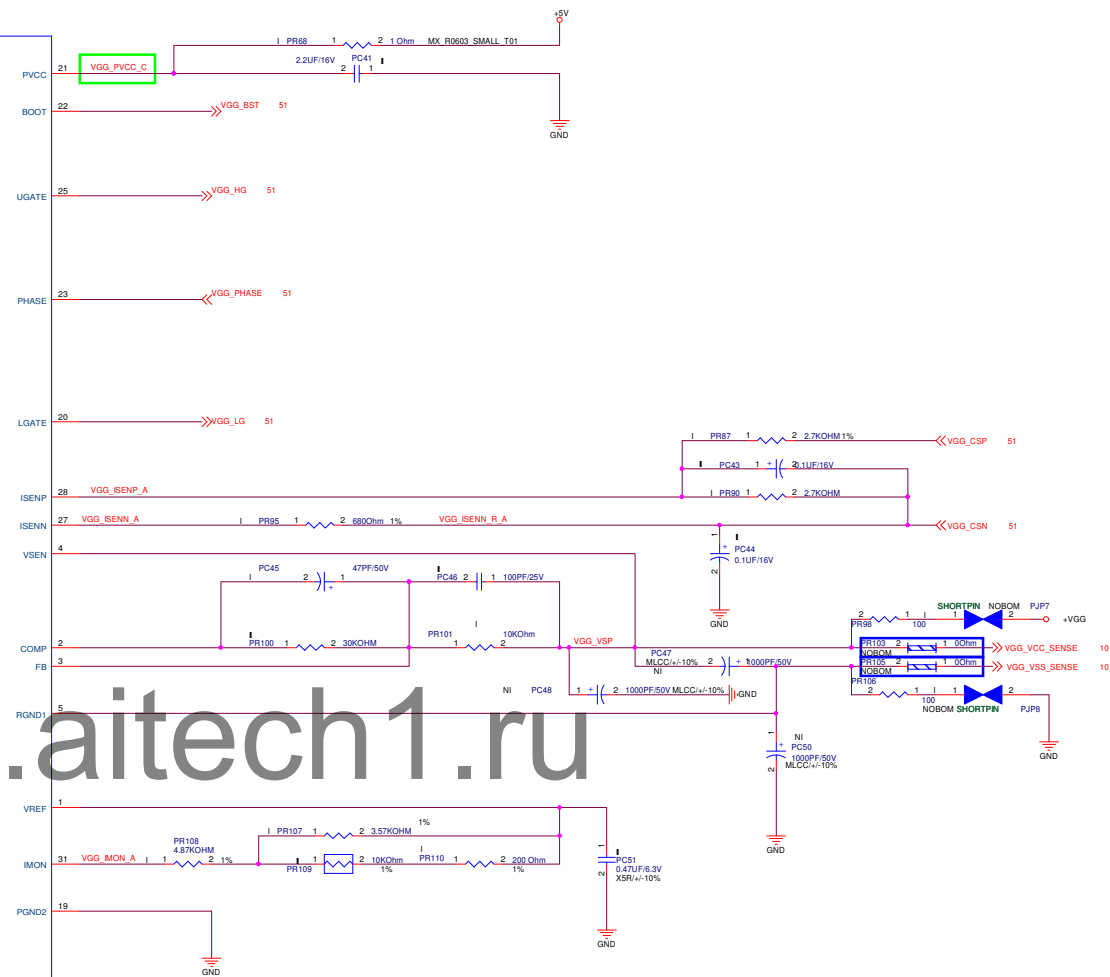
+VCC0/ Max:7A / TDC:4.9A



Owner	Worst case	Low Limit	High Limit
zIVO	14A	TBD	32A
ChenYang			

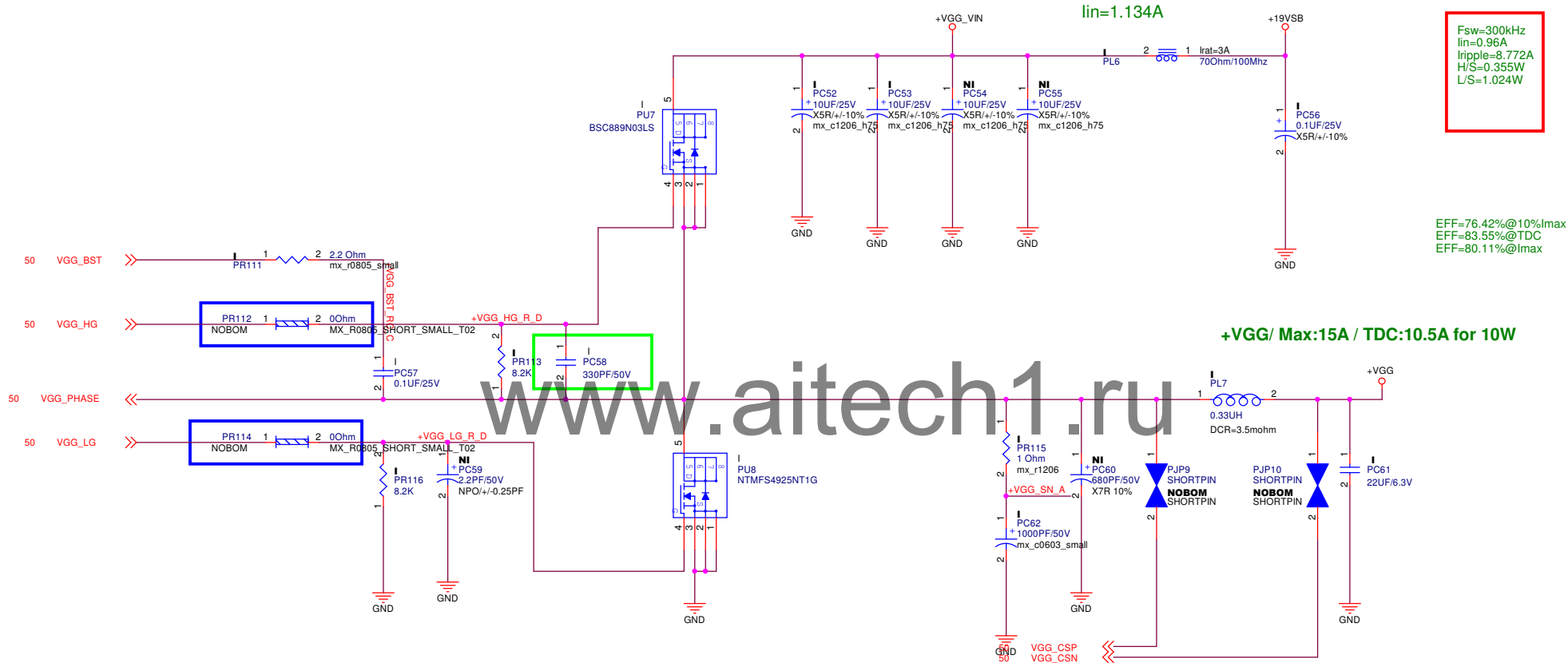
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Title		
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Size A3	Document Number IPMBW-BR	Rev R1.09
Date: Wednesday, May 13, 2015	Sheet 49	of 85



Title			
<Title>			
Size A2	Document Number IPMBW-BR		Rev R1.00
Date:	Wednesday, May 13, 2015	Sheet	50 of 85

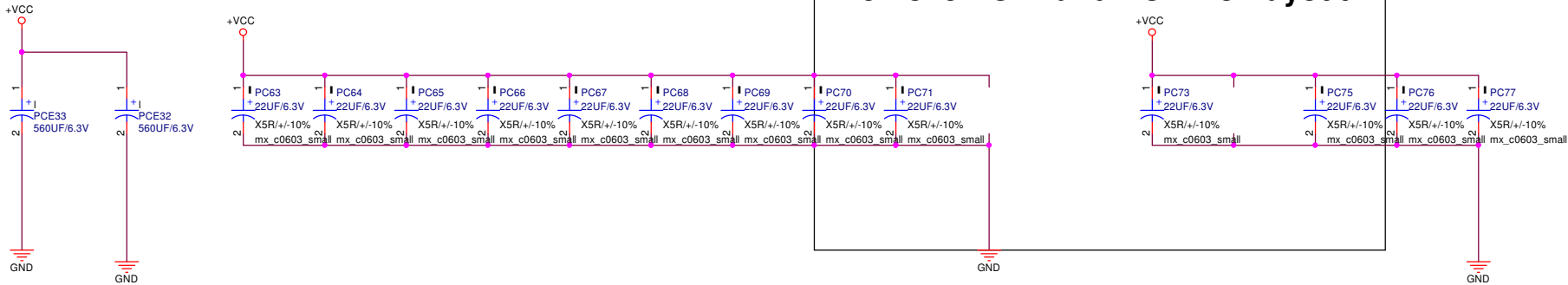
+VGG, PLACE NEAR CPU



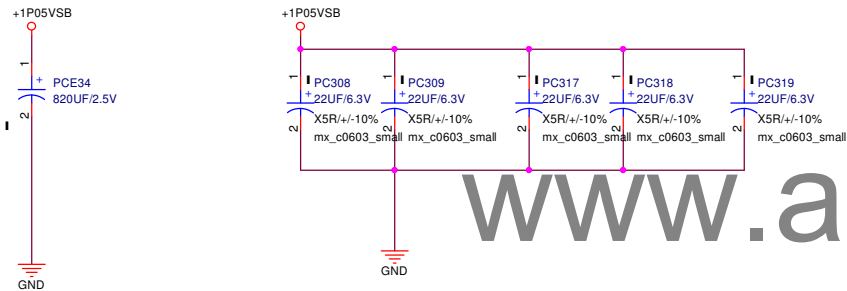
Owner	Worst case	Low Limit	High Limit
ZIVO	22.5A	TBD	32A
ChenYang			

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Size	Document Number		Rev
A3	IPMBW-BR		R1.08
Date:	Wednesday, May 13, 2015		Sheet 51 of 85

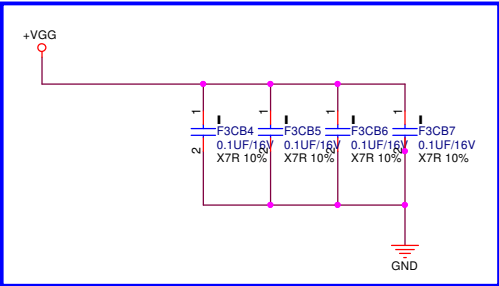
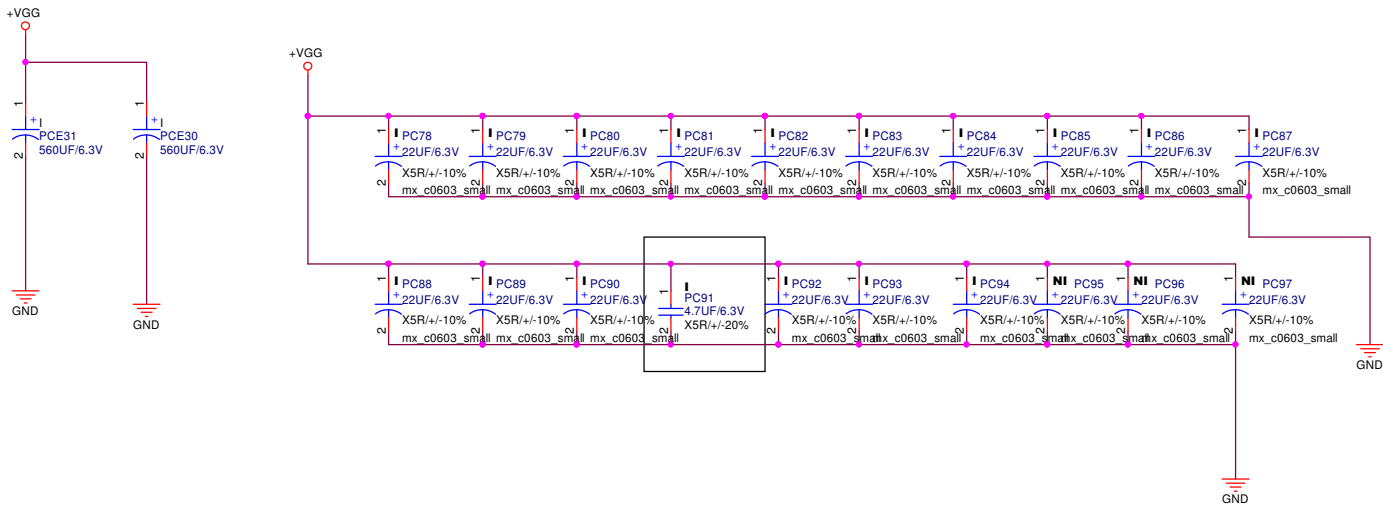
+VCC0 Output CAP



+VNN Output CAP

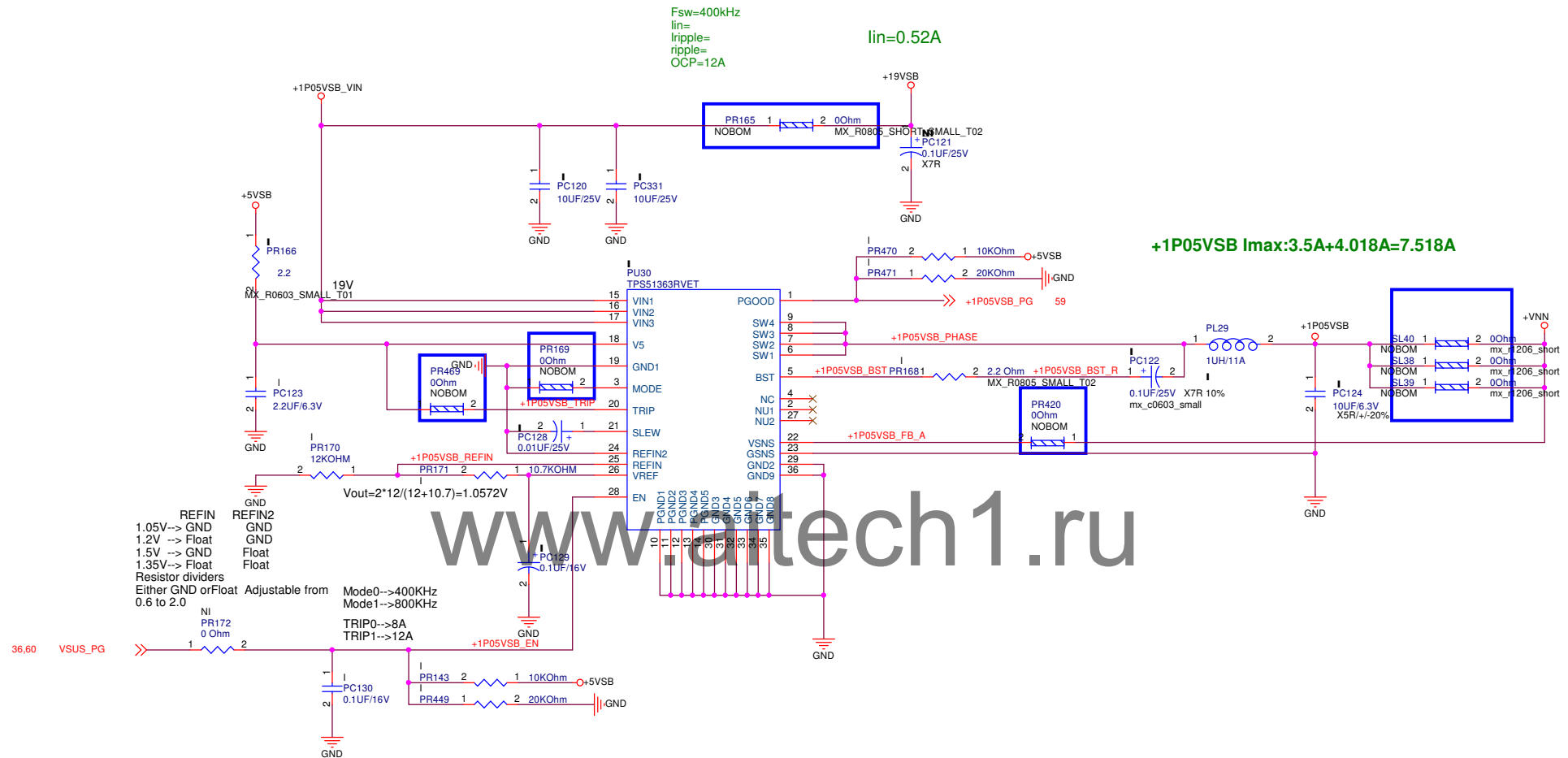


+VGG Output CAP



Cross Moart Cap

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Size	Document Number		Rev
A3	IPMBW-BR		R1.08
Date:	Wednesday, May 13, 2015	Sheet	52 of 85



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PEGATRON Title : **+1P05VSB**

PEGATRON CORPORATION Engineer: **CK_Lee**

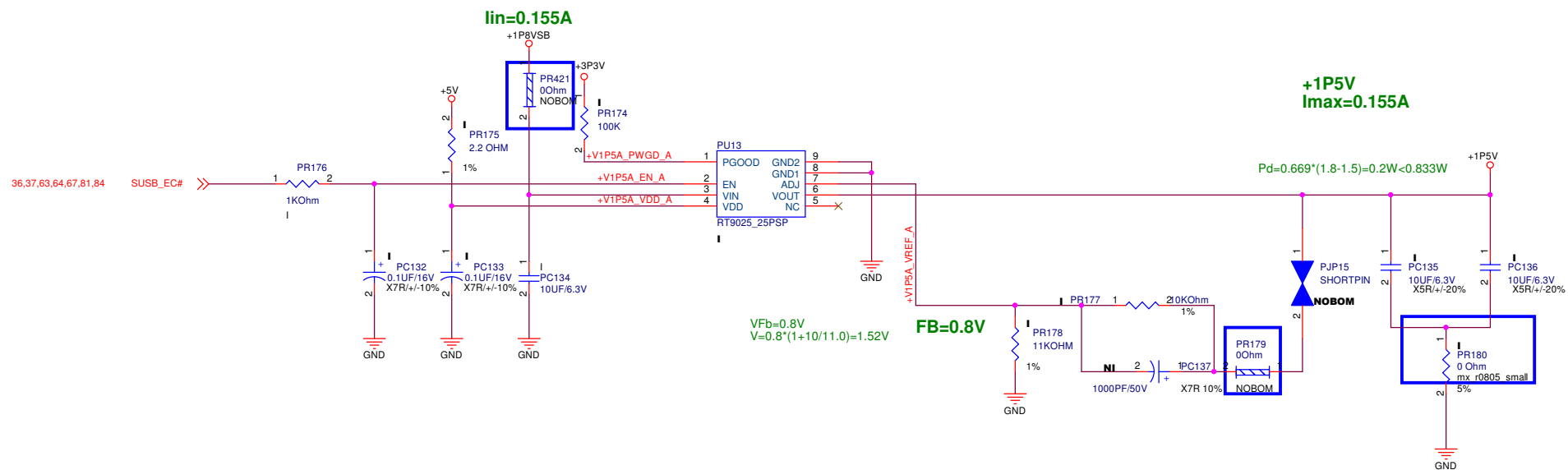
Size	Project Name	Rev
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Size	Document Number		Rev
A3	IPMBW-BR		R1.00
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Date:	Wednesday, May 13, 2015		Sheet 55 of 85



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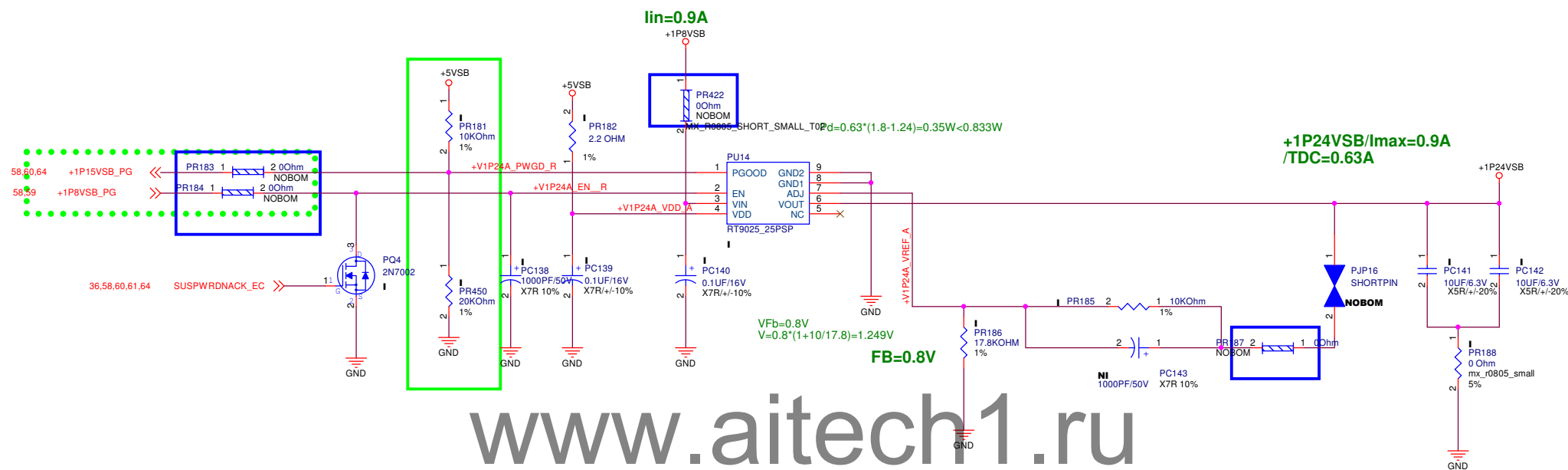
Size
A3

Document Number
IPMBW-BR

Date: Wednesday, May 13, 2015

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Rev
R1.08



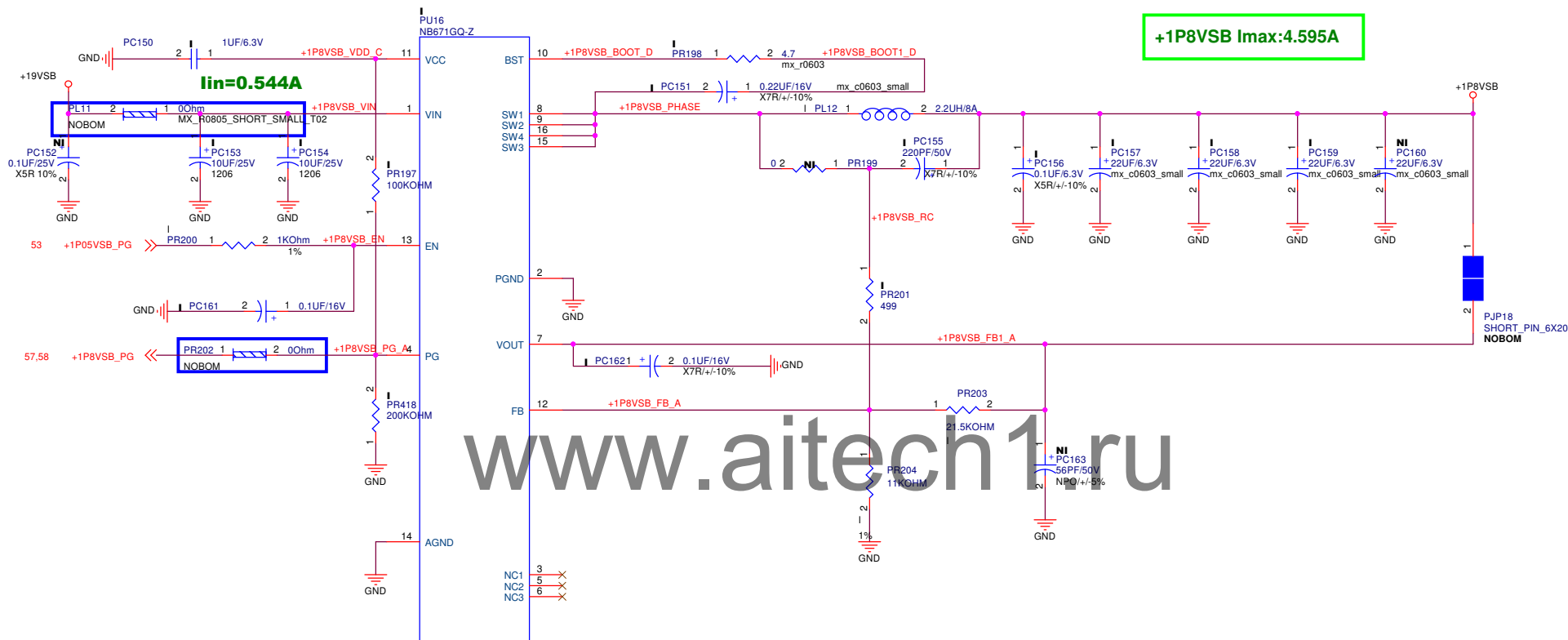
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Size A3 Document Number
IPMBW-BR

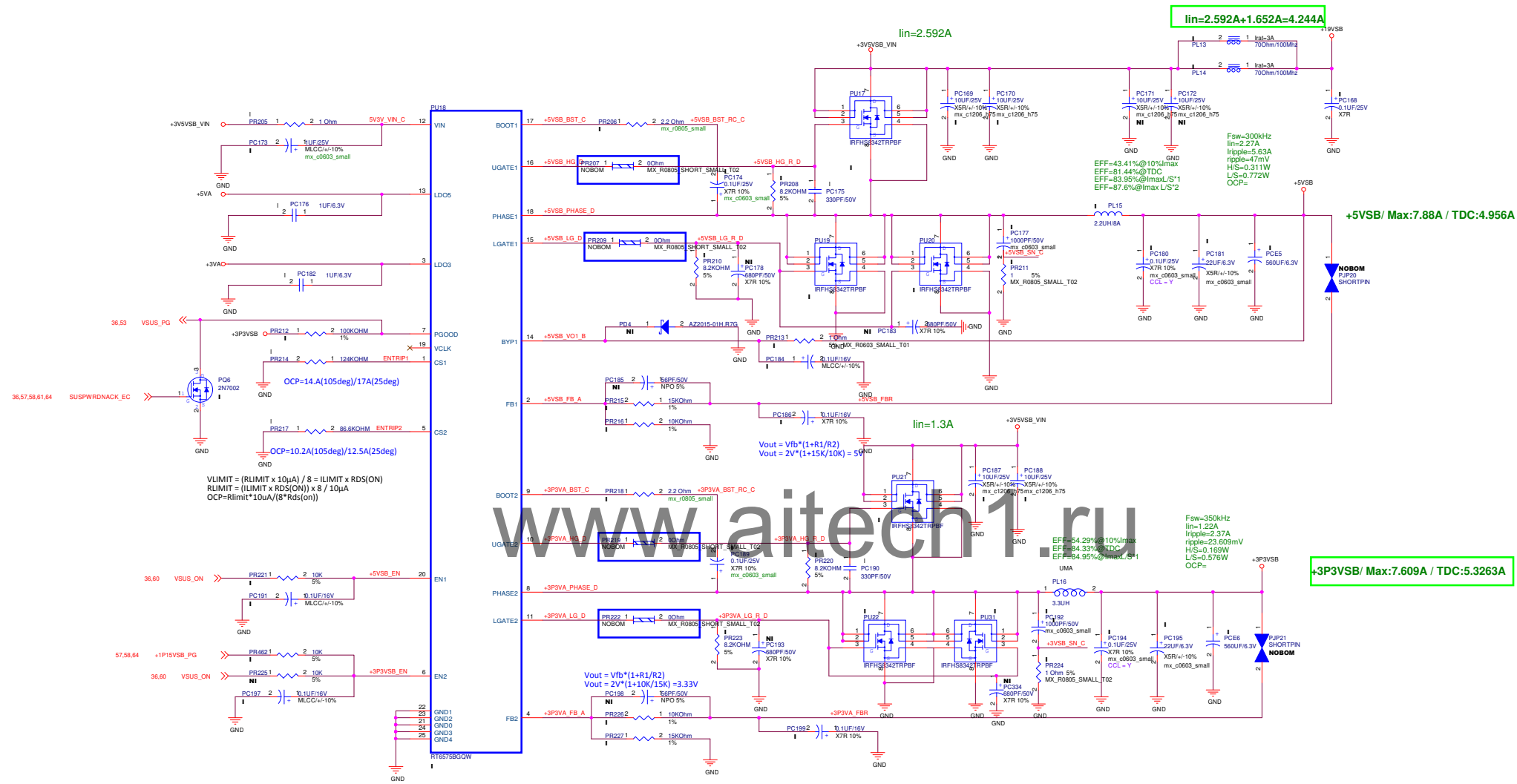
Rev
R1.08

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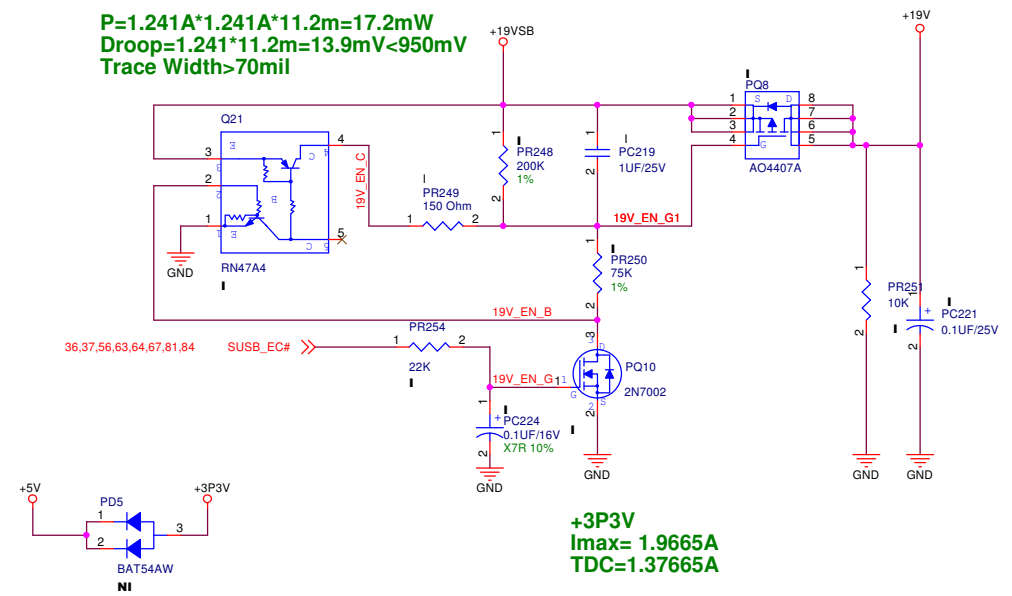
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Date:	Wednesday, May 13, 2015	Sheet 59 of 85

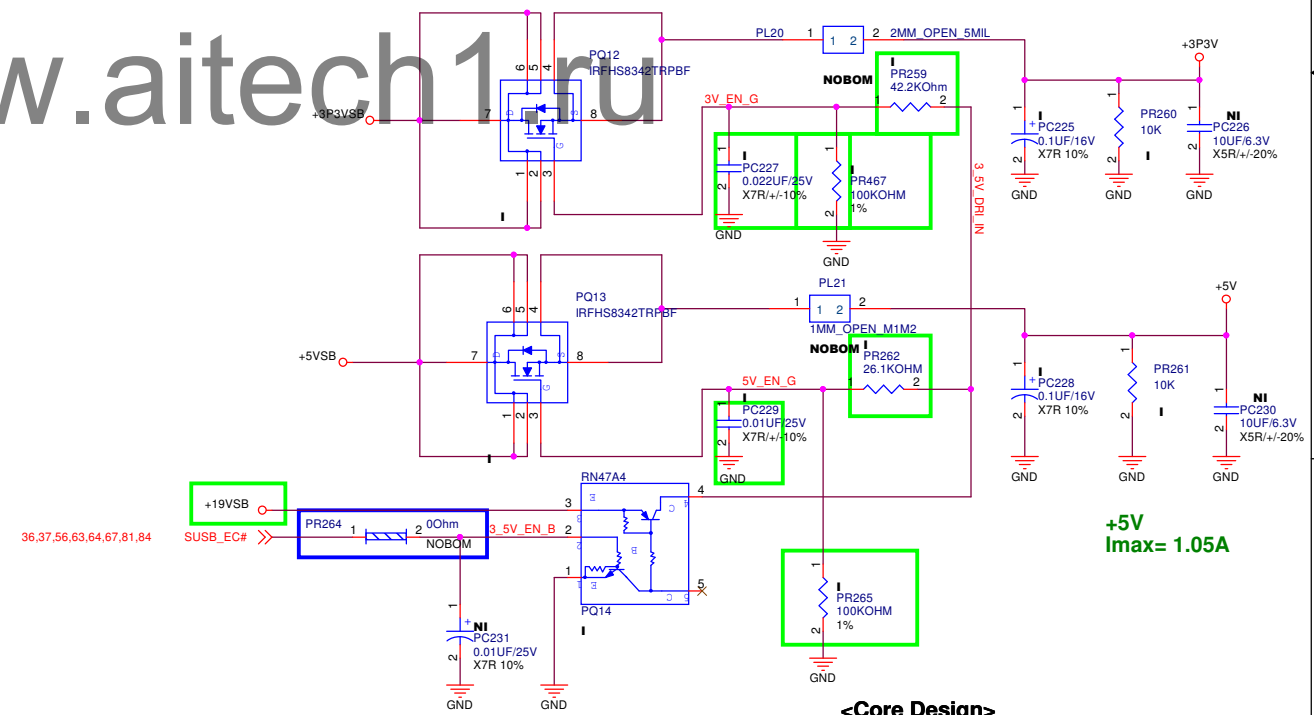


+19VSB ==> +19V
I_{max}= ??A

$P=1.241A \times 1.241A \times 11.2m=17.2mW$
 $\text{Droop}=1.241 \times 11.2m=13.9mV < 950mV$
Trace Width > 70mil



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<Core Design>		
PEGATRON		
Title : Power Sequence		
PEGATRON CORPORATION		
Engineer: CK_Lee		
Size	Project Name	Rev
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Date: Wednesday, May 13, 2015		
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+1P8V
 $I_{max}=0.09A$
 $TDC=0.063A$
 $Trace\ Width>30mil$
 $P=0.063A*0.063*41.5mohm=0.163mW$
 $Drop=0.063A*41.5mohm=2.61mV<90mV$

+1P05V
 $I_{max}=0.078A$
 $Trace\ Width>20mil$
 $P=0.078A*0.078*41.5mohm=0.252mW$
 $Drop=0.063A*41.5mohm=3.237mV<52.5mV$

+5V_LCD
 $I_{max}=1.65A$
 $TDC=1.16A$
 $Trace\ Width>30mil$
 $P=1.16A*1.16*24mohm=32.3mW$
 $Drop=0.063A*24mohm=27.8mV<250mV$

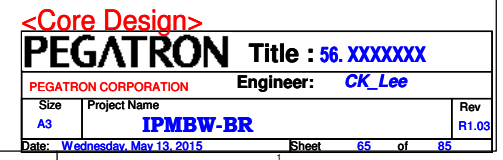
+3P3VSB_PRIME
 $I_{max}=0.68A$
 $TDC=0.48A$
 $Trace\ Width>30mil$
 $P=0.48A*0.48*41.5mohm=9.56mW$
 $Drop=0.48A*41.5mohm=19.9mV<165mV$

57,58,60 +1P15VSB_PG

36,57,58,60,61 SUSPWRDNACK_EC

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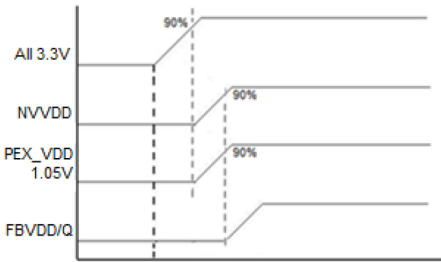
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Size	Document Number		Rev
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Imax= 5.86A
TDC=3.38A
Trace Width>150mil

Droop: $4.23\text{A} \cdot 8.5\text{m}\Omega = 36\text{mV} < 40.5\text{mV}$

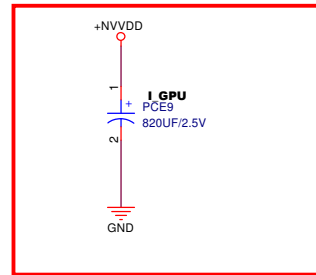
```
+PEXVDD(1.05V)
Trace Width>30mil
P=1.553A*1.553A*7.5mohm=18mW @VGS=10V
Droop:2.29A*7.5mohm=17.175mV<31.5mV(+/-3%) @VGS=10V
```



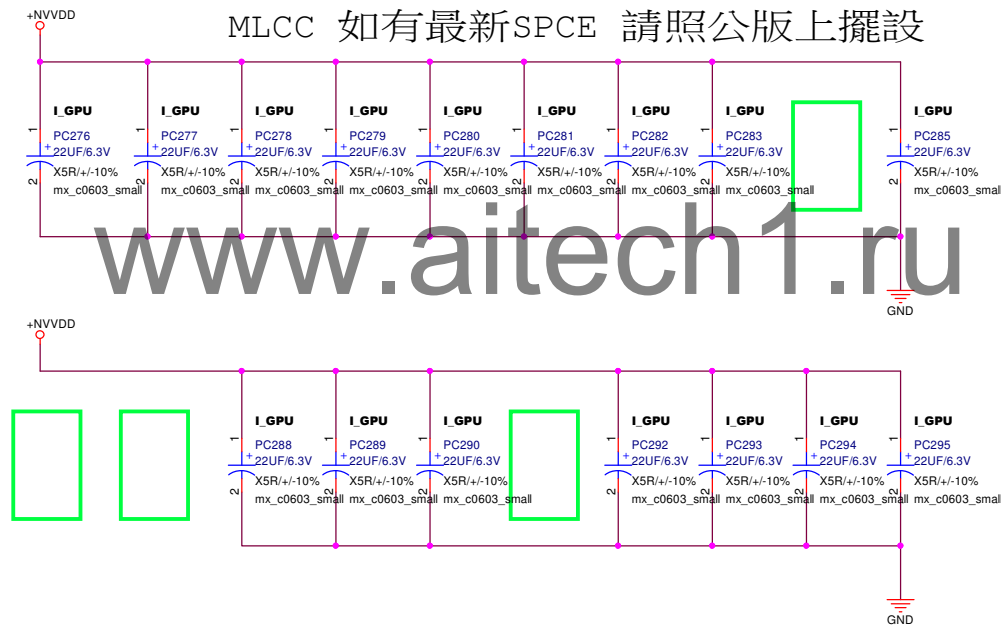
Notes: - All 3.3V includes all rails powered at 3.3V
- PEX_VDD 1.05V includes all rails that are shared

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Title <Title>			
Size A3	Document Number IPMBW-BR		Rev R1.08
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Power VR 輸出端



MLCC 如有最新SPCE 請照公版上擺設



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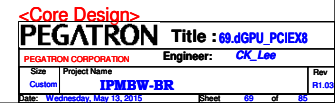
PEGATRON Title : 56. XXXXXX

PEGATRON CORPORATION Engineer: CK_Lee

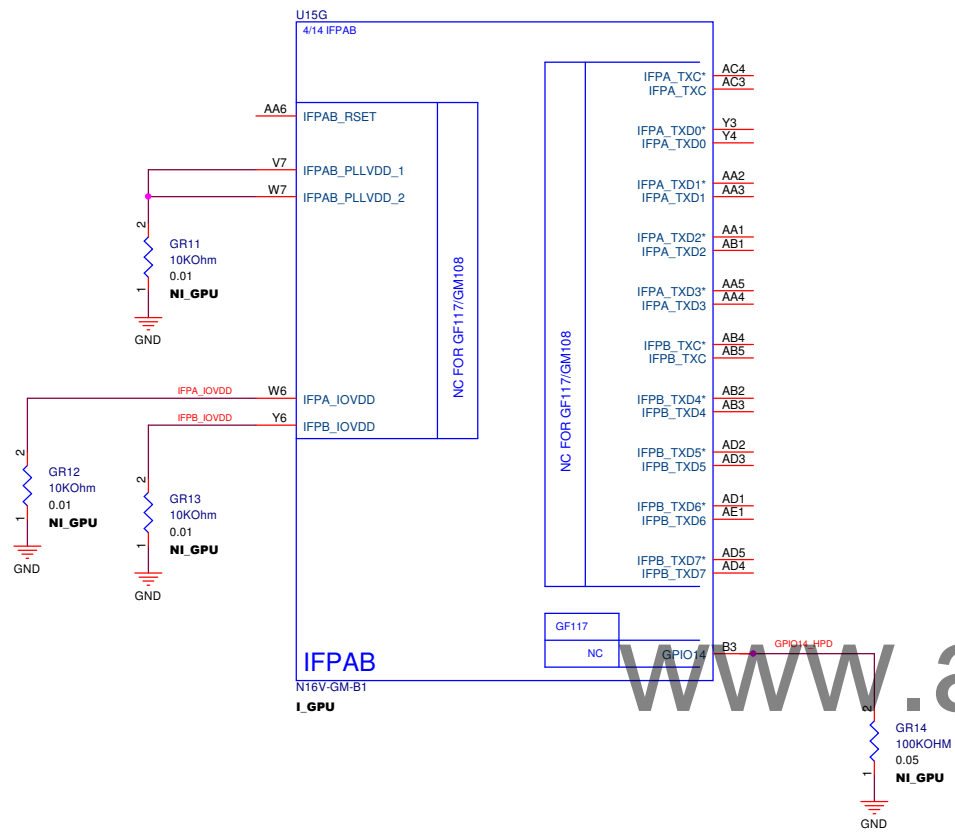
Size A3	Project Name IPMBW-BR	Rev R1.03
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R1.01-2012/09/26:add C9972 220pf "NI" for GPU "PCIE_RST#"
R1.01-2012/09/28: For GPU PCIE_WAKE#,Add NR132 0ohm for switch.



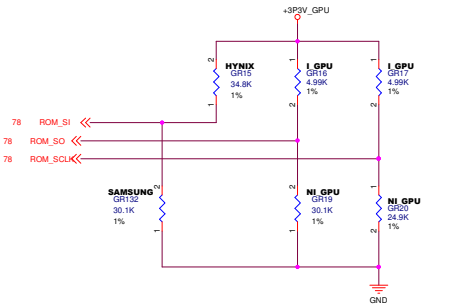
IFPA/B LVDS Dual Link



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Straps Mapping

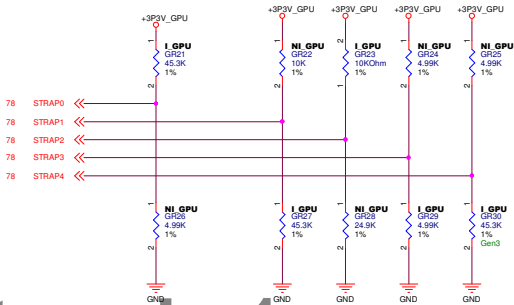
Will need to check and follow the update in PUN									
N16V-GM-S DID0x1299 10011001									
	ROM_SCL	1	1	0	0	PU	24.9Kohm	1%	
	ROM_SI	1	1	1	0	PU	4.99Kohm	1%	
	ROM_SO	0	1	0	1	PD	34.8Kohm	1%	
	STRAP0	1	0	0	0	PU	30.1Kohm	1%	
	STRAP1	1	1	1	1	PU	4.99Kohm	1%	
	STRAP2	0	1	1	1	PD	45.3Kohm	1%	
	STRAP3	1	0	0	1	PU	45.3Kohm	1%	
	STRAP4	0	0	0	0	PD	10Kohm	1%	
	STRAP4	0	1	1	1	PD	4.99Kohm	1%	
	STRAP4	0	1	1	1	PD	45.3Kohm	1%	



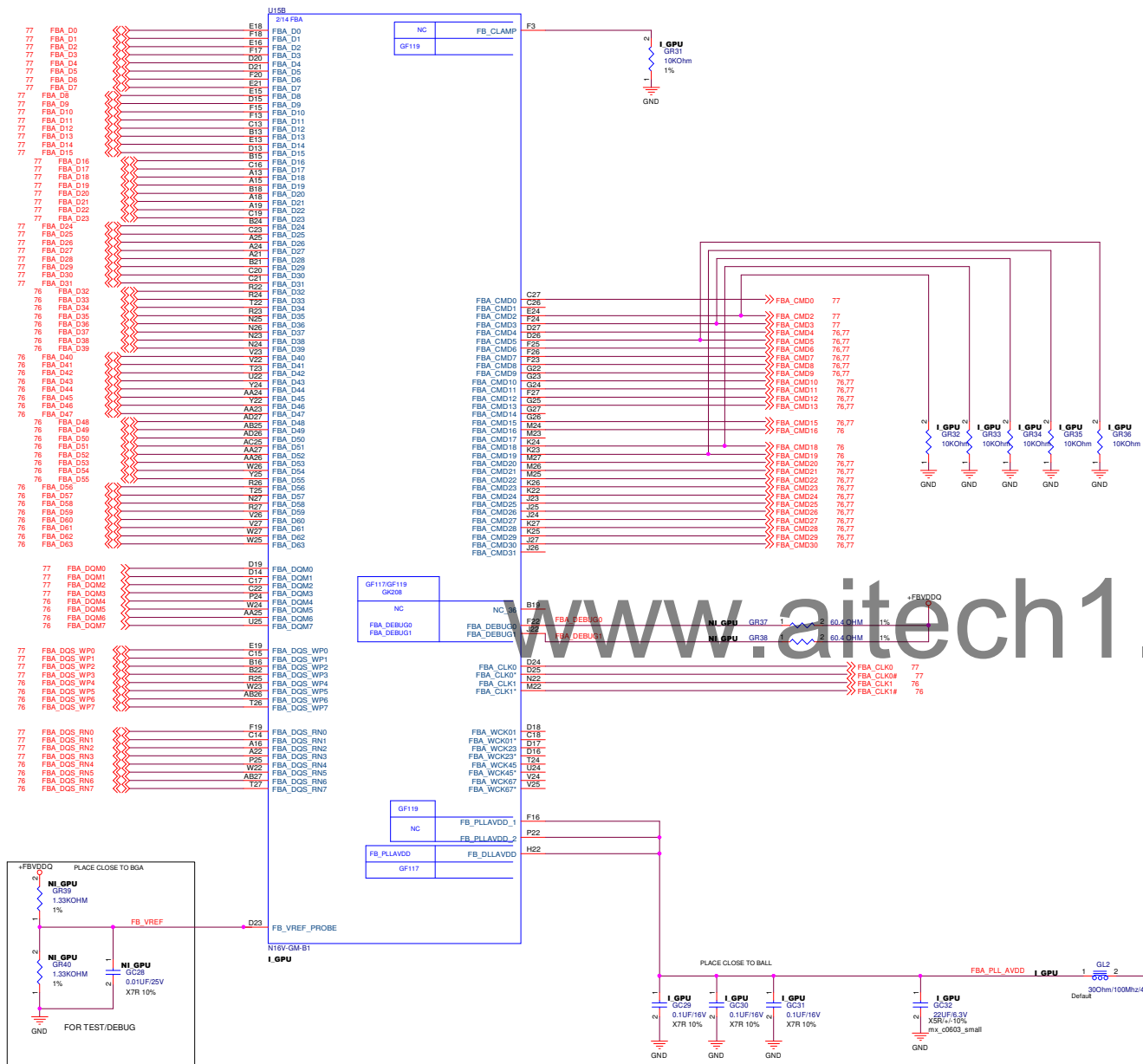
Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0	Resistor Values	Pull-up to VDD33	Pull-down to GND
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM	4.99 kΩ	1000	0000
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]	10.0 kΩ	1001	0001
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE	15.0 kΩ	1010	0010
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	20.0 kΩ	1011	0011
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	24.9 kΩ	1100	0100
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	30.1 kΩ	1101	0101
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	34.8 kΩ	1110	0110
STRAP4	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V	45.3 kΩ	1111	0111

Table 2. N16V-GM DDR3L Recommended Memories

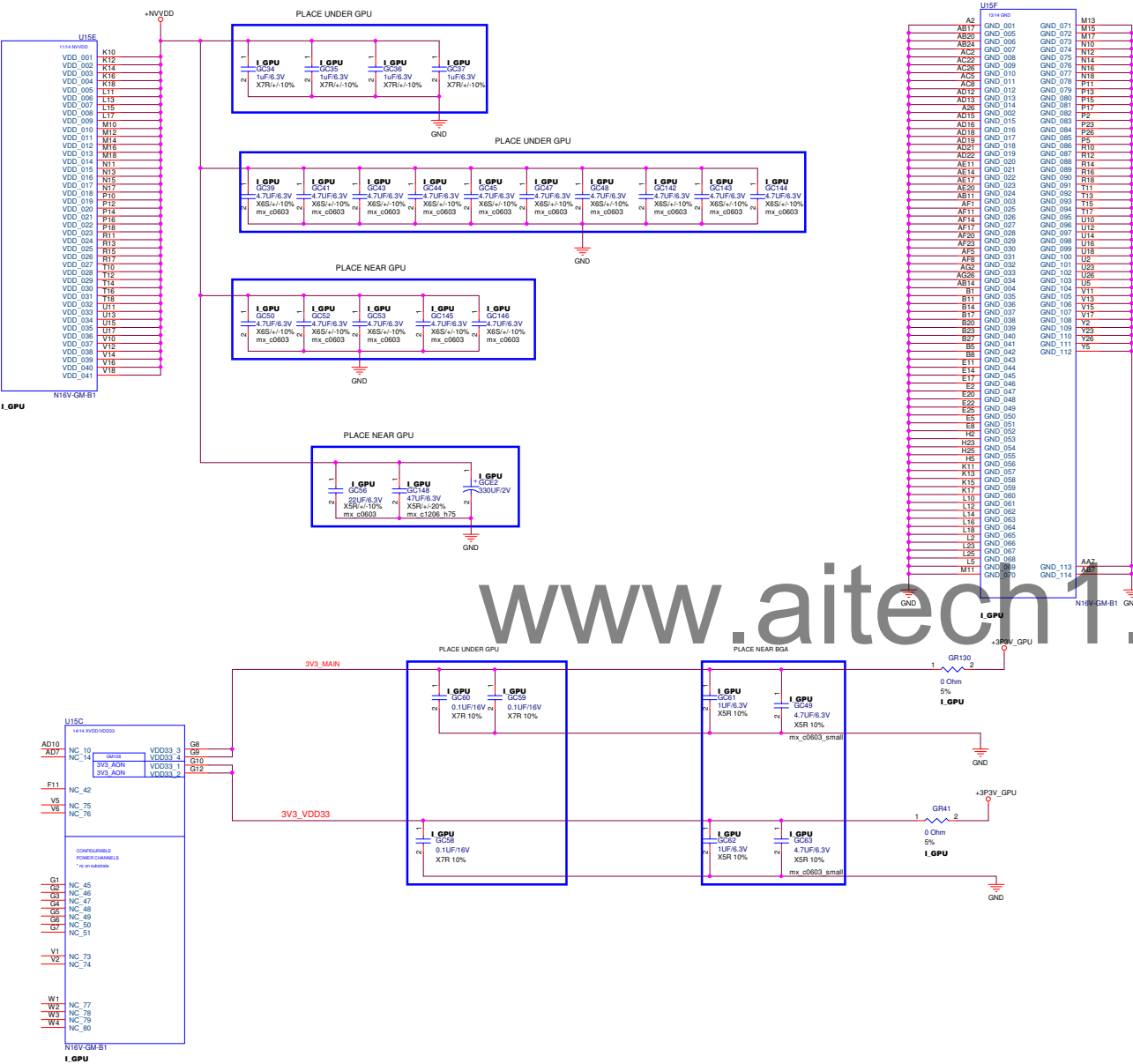
Memory Type	FBVDD/ FBVDDQ	Memory Density	Configuration	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed CK Grade(MHz)	Memory Date Code Minimum	Status
DDR3L	1.35V/ 1.35V	128Mx16	Single Rank or Single Rank Stuffing for Dual Rank	Hynix	H5TC2G63FR-11C	F-die	0x8	900	N/A	Production candidate
				Micron	MT41J128M16JT-093G-K	K-die	0x8	900	1322	Production candidate
				Samsung	K4V2G1646Q-BC1A	Q-die	0x7	900	N/A	Production candidate
		256Mx16	Single Rank or Single Rank Stuffing for Dual Rank	Hynix	H5TC4G63AFR-11C	A-die	0xE	900	N/A	Production candidate
				Micron	MT41J256M16HA-093G-E	E-die	0xD	900	1322	Production candidate
				Samsung	K4V4G1646D-BC1A	D-die	0x5	900	N/A	Production candidate
			Dual Rank	Hynix	H5TC4G63AFR-11E	A-die	0xE	900	N/A	Production candidate
				Micron	MT41J256M16HA-093G-E	E-die	0xD	900	1322	Production candidate
				Samsung	K4V4G1646D-BC1A	D-die	0x5	900	N/A	Production candidate



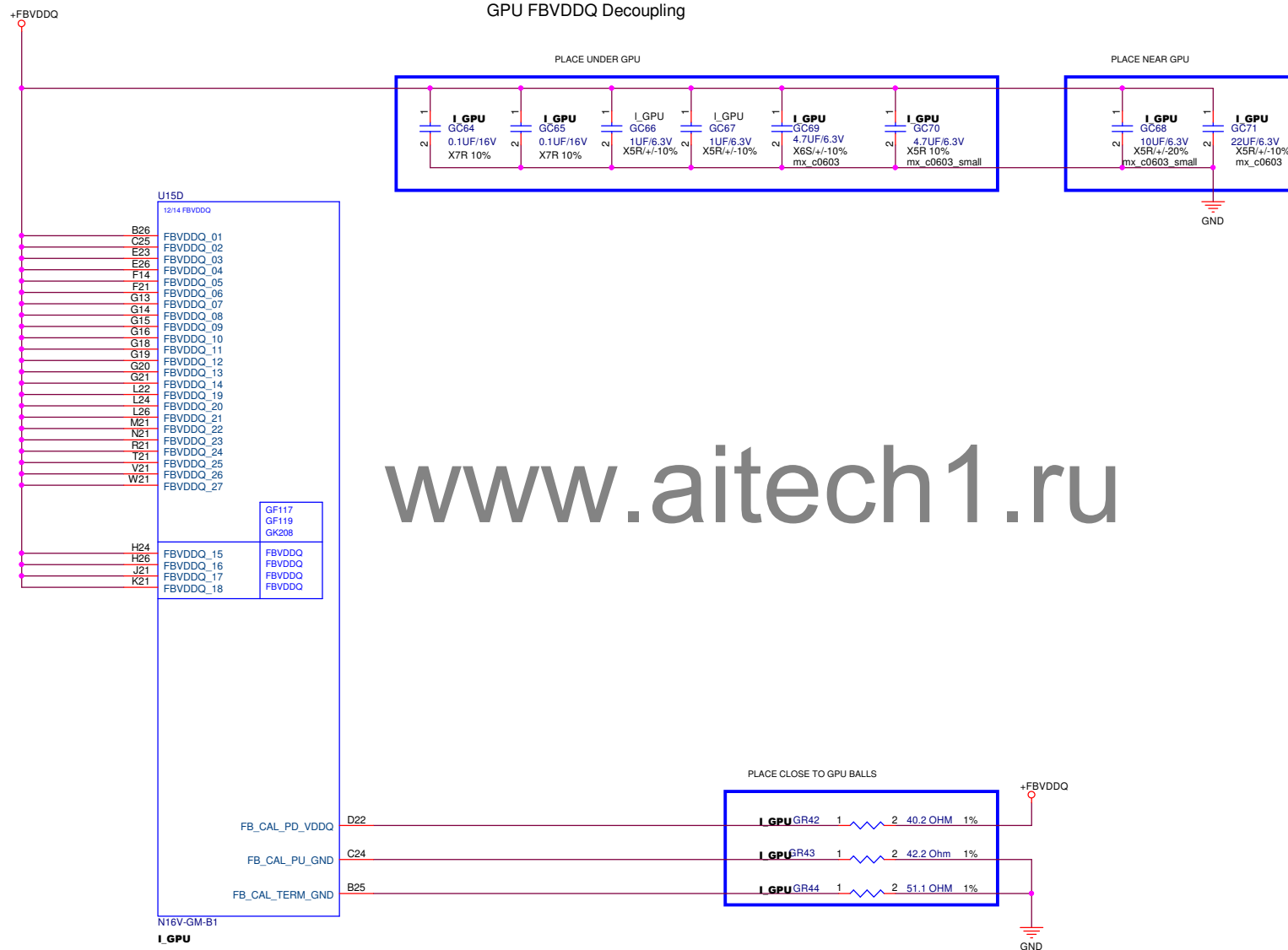
Frame Buffer Partitions A/B



Power/Decoupling: +NVVDD,3V3_NV,GRND,and Optional



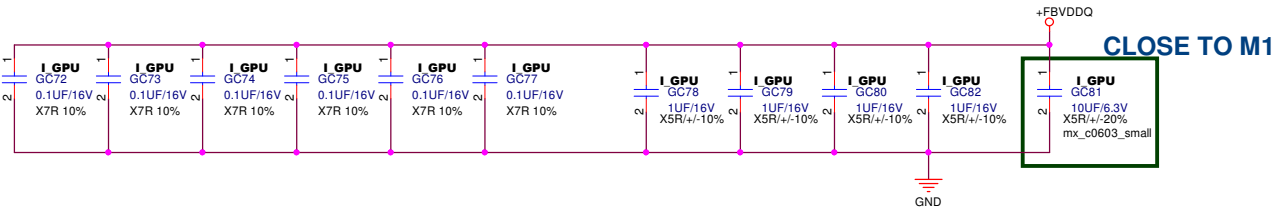
Frame Buffer FBVDDQ Power/Decoupling/Calibration



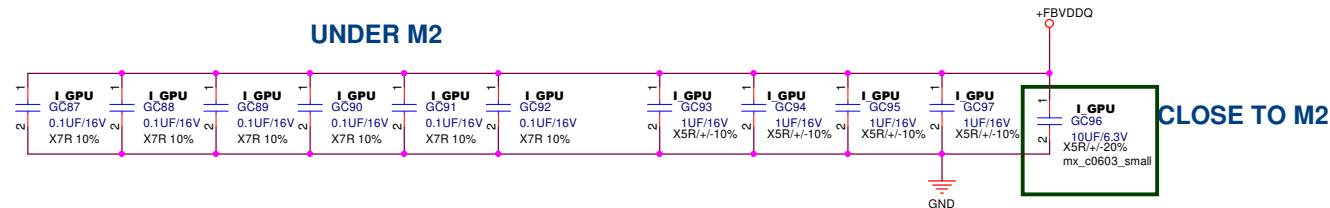
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Memory FBVDD/Q Decoupling

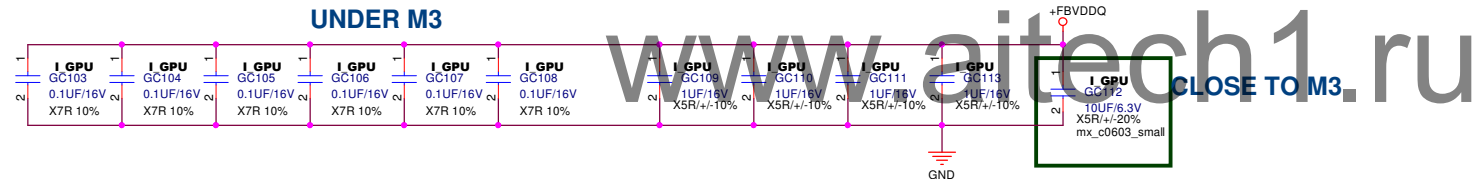
UNDER M1



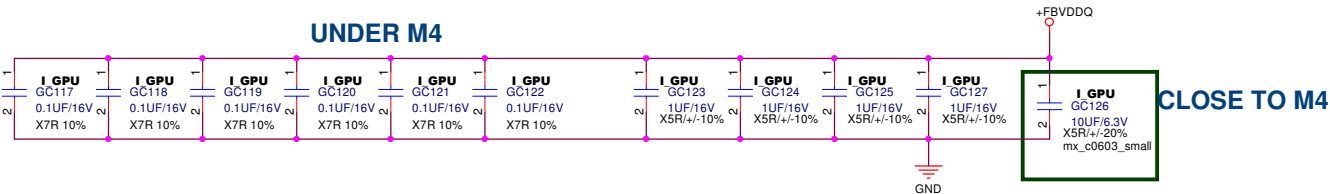
UNDER M2



UNDER M3

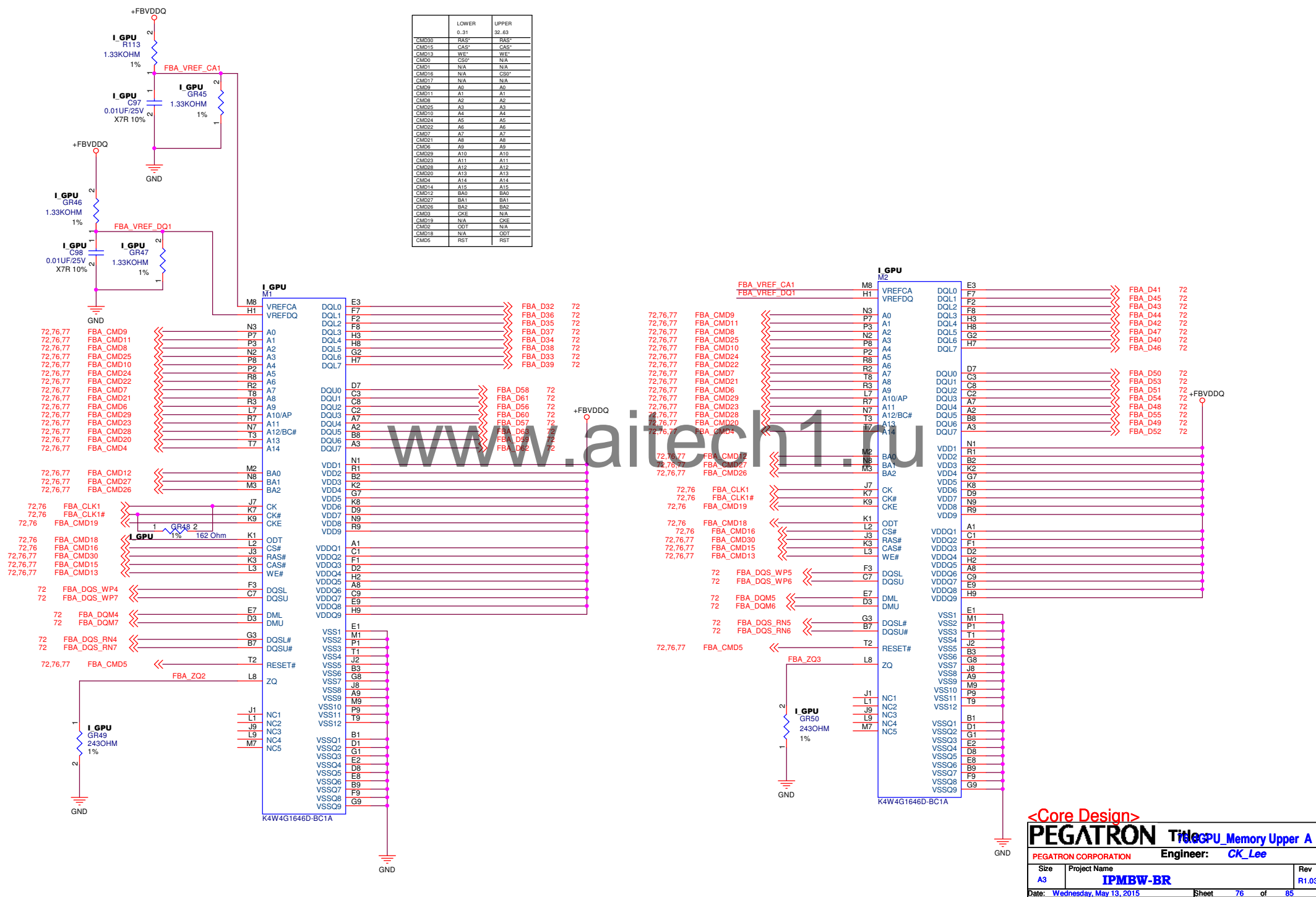


UNDER M4



Memory Upper Partition A

	LOWER	UPPER
	0.31	32.63
CM010	BAS ^a	BAS ^a
CM015	GAS ^a	GAS ^a
CM013	WE ^b	WE ^b
CM00	CSO ^c	N/A
CM01	N/A	N/A
CM016	N/A	CSO
CM07	N/A	N/A
CM011	A1	A1
CM08	A2	A2
CM05	A3	A3
CM010	A4	A4
CM04	A5	A5
CM022	A6	A6
CM07	A7	A7
CM021	A8	A8
CM06	A9	A9
CM028	A10	A10
CM023	A11	A11
CM028	A12	A12
CM02	A13	A13
CM04	A14	A14
CM012	A15	A15
CM019	BA0	BA0
CM027	BA1	BA1
CM026	BA2	BA2
CM03	C0E	N/A
CM019	N/A	C0E
CM02	C0T	N/A
CM018	N/A	C0T
CM05	RST	RST



	LOWER	UPPER
	6.31	32.63
CM030	RAS ^a	RAS ^a
CM055	CAS ^a	CAS ^a
CM016	WE ^b	WE ^b
CM01	CSO ^c	N/A
CM01	N/A	N/A
CM013	N/A	CSO ^c
CM017	N/A	N/A
CM09	A0	A0
CM011	A1	A1
CM012	A2	A2
CM025	A3	A3
CM010	A4	A4
CM014	A5	A5
CM022	A6	A6
CM07	A7	A7
CM018	A8	A8
CM06	A9	A9
CM029	A10	A10
CM015	A11	A11
CM028	A12	A12
CM020	A13	A13
CM014	A14	A14
CM014	A15	A15
CM022	BA0	BA0
CM012	BA1	BA1
CM03	BA2	BA2
CM03	CKE ^d	N/A
CM019	N/A	CKE ^d
CM02	DOT	DOT
CM018	N/A	DOT
CM05	RST	RST



BIOS, External SS, and Mechanical Components

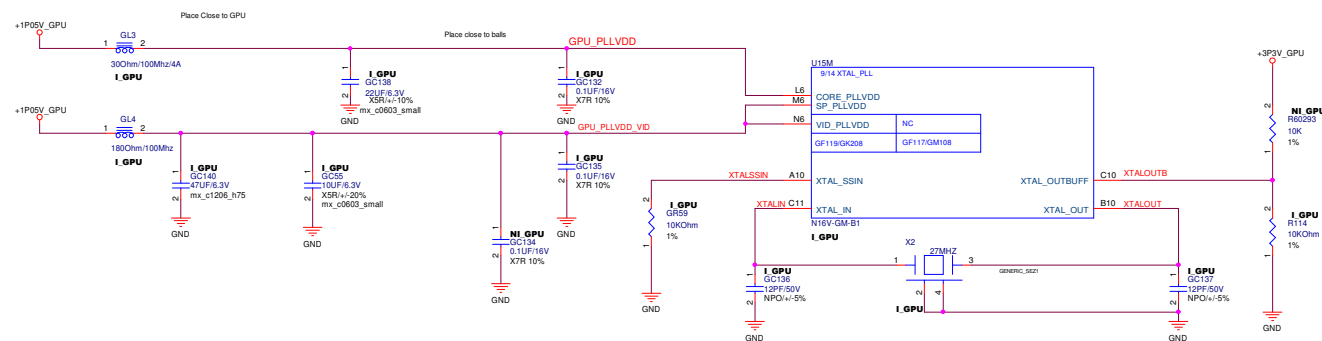
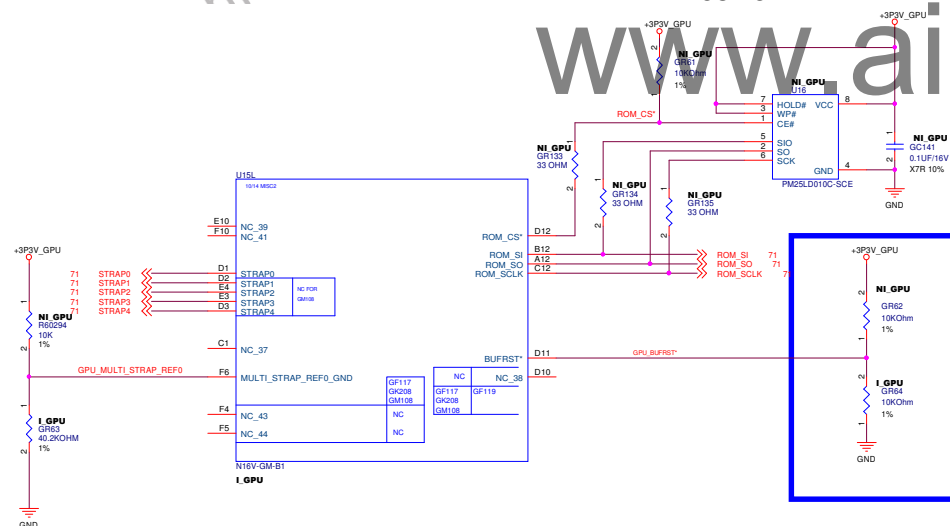


Table 119. Device Specific Strap Mode Selection

	N14M-GE/-GL	Other N14x GPUs
Multi_Strap_Ref2_GND (Only on GB2-64 package)	No Connect	N/A
Multi_Strap_Ref1_GND (Only on GB2-64 package)	No Connect	N/A
Multi_Strap_Ref0_GND	No Connect	40.2k 1% to GND
Strap Mode Selected	Binary	Multi-Level

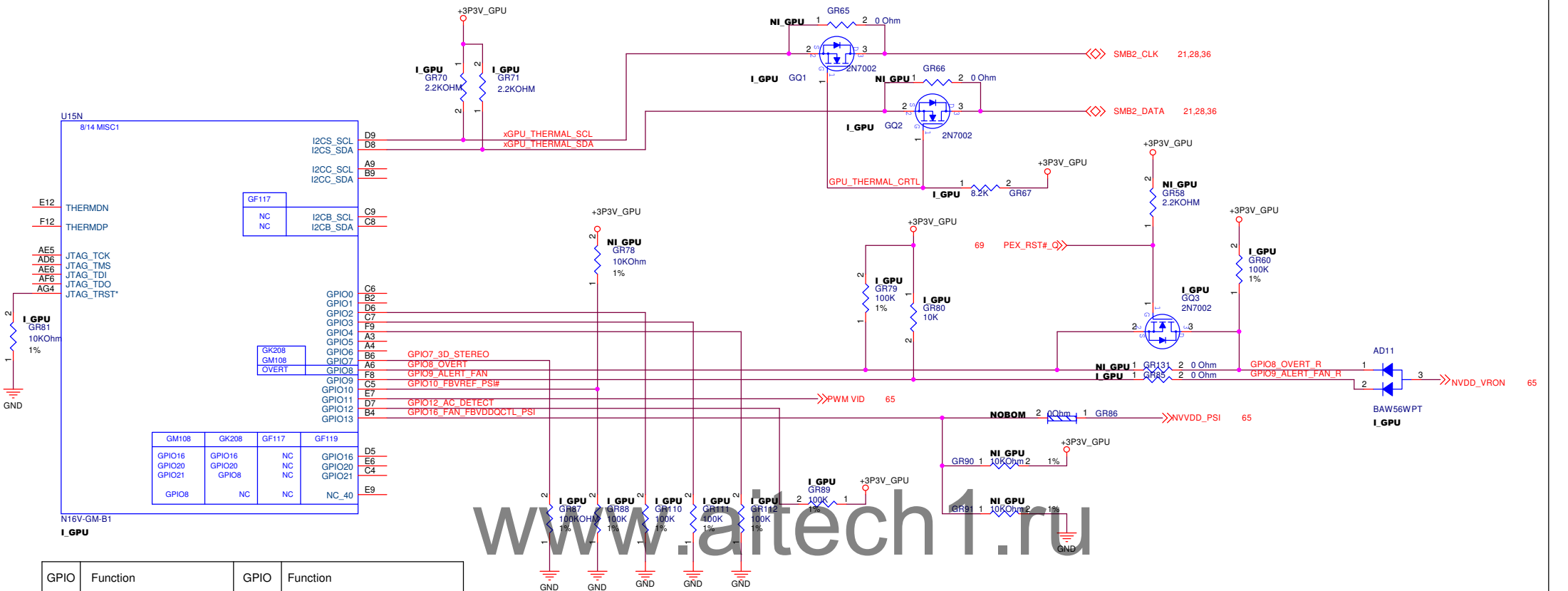
STUFF PDs on XTALSSIN and
XTALOUTBUFF WHEN EXT_SS
IS NOT USED

BIOS ROM



R1.01-2011/12/22:
Add R37589 to pull down;
R37586 change to "NI".

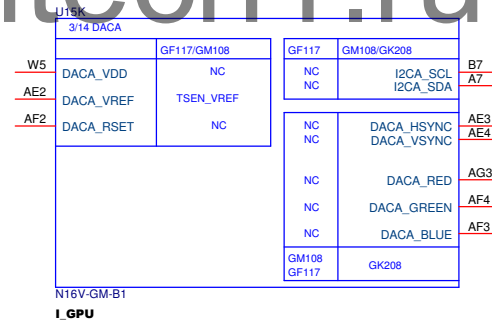
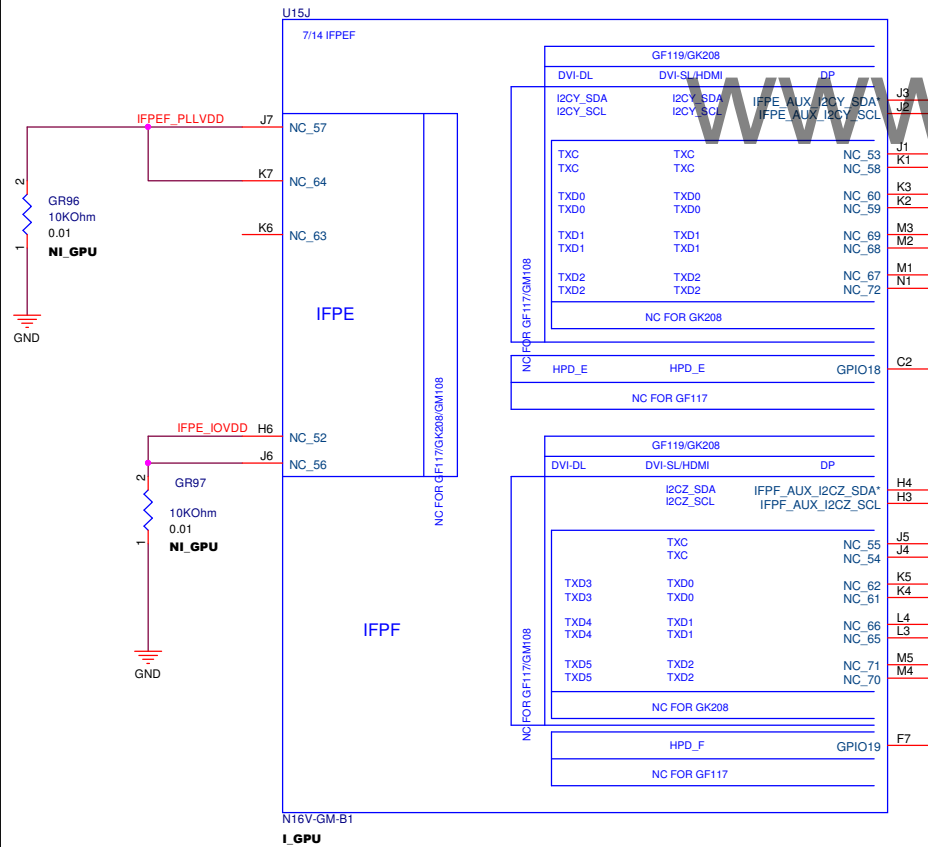
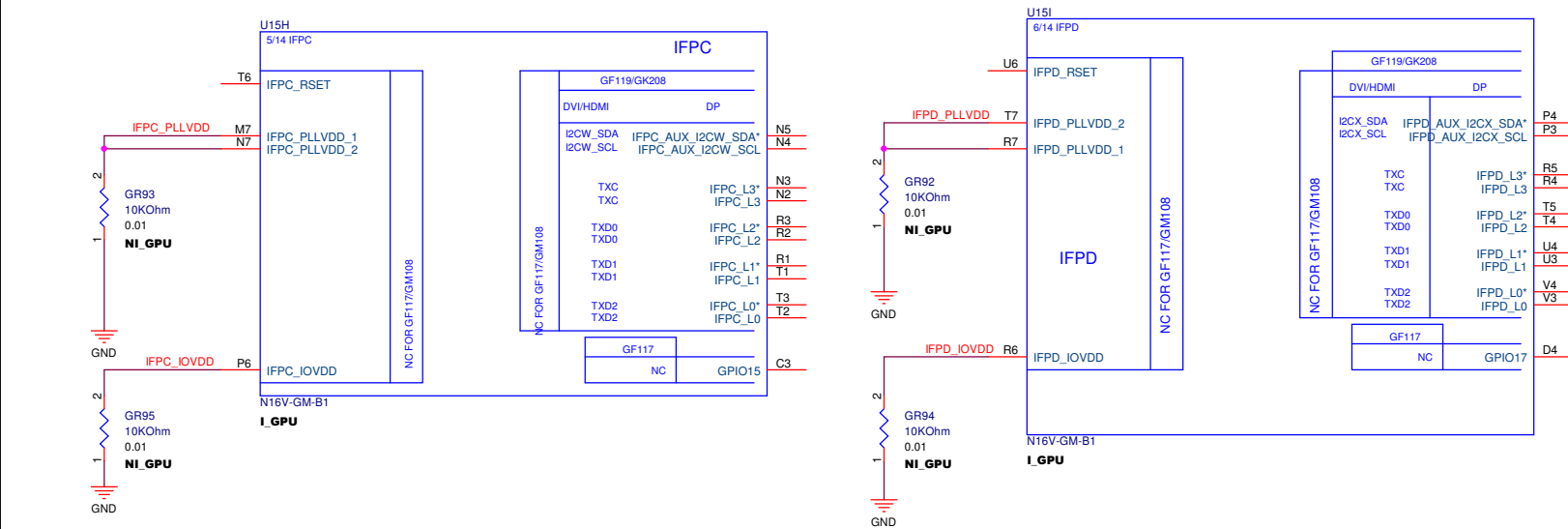
GPIOs, Thermal Sensor, I2C/GPIO Expanders



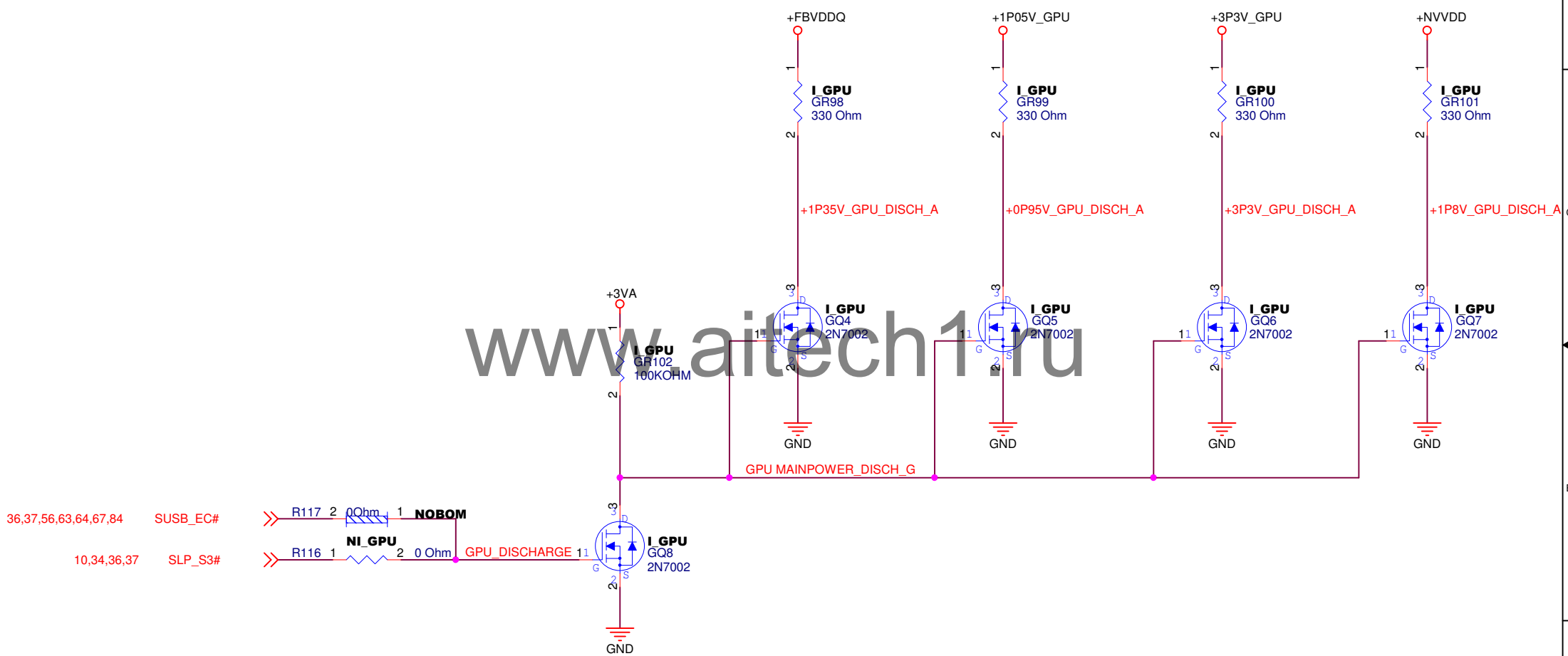
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GPIO	Function	GPIO	Function
GPIO 0	Debug/Service Header/Alt_Fan PWM	I2C PORT C	
GPIO 1	VID 2	EXPND 0	Level Shifter Error Correction
GPIO 2	LCD brightness control (BL PWM)	EXPND 1	NVGEM GPIO EXP1/ PS_Margin*
GPIO 3	LCD Power enable (PPEN)	EXPND 2	NVGEM GPIO EXP2/PS_MR*
GPIO 4	LCD Backlight enable (BLEN)	EXPND 3	GPIO_DEBUG_SERVICE HEADER
GPIO 5	VID 0		
GPIO 6	VID 1		
GPIO 7	3D STEREO		
GPIO 8	GPU Overtemp	EXPND 4	GPU_PS_EN
GPIO 9	GPU thermal Alert	EXPND 5	RSVD
GPIO 10	FB Vref Control (not used sDDR3)	EXPND 6	PEX_RST
GPIO 11	FBVDD/Q VID (Reserved)	EXPND 7	RSVD
GPIO 12	PWR_Level AC Detect		
GPIO 13	PS1 Vprgm Enable		
GPIO 14	HPD for IFP AB (not used)		
GPIO 15	HPD for IFP C (HDMI/DP)		
GPIO 16	Fan PWM control		
GPIO 17	HPD for IFP D (DP)		
GPIO 18	HPD for IFP E (DVI-I DL)		
GPIO 19	HPD for IFP F (not used)		
GPIO 20	NVGEM Debug GPIO13		
GPIO 21	NVGEM Debug GPIO14		

IFPD DUAL MODE DP HDMI DVI



GPU POWER DISCHARGE



<Core Design>

PEGATRON Title : 81.GPU POWER DISCH

PEGATRON CORPORATION Engineer: CK_Lee

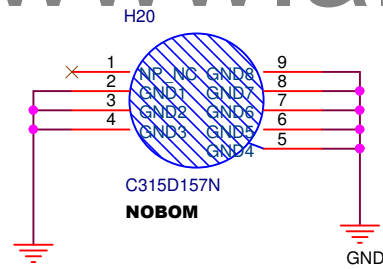
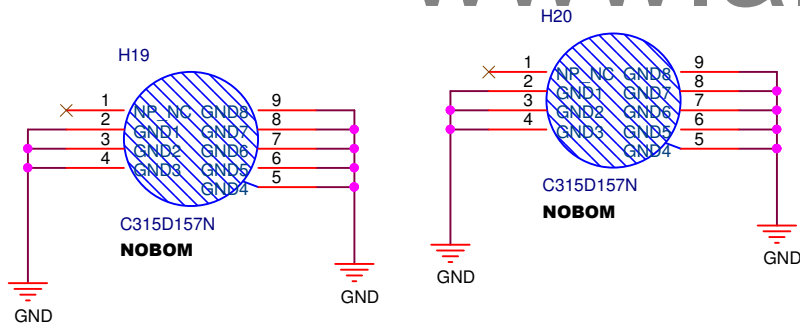
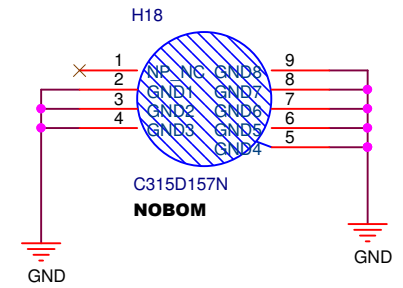
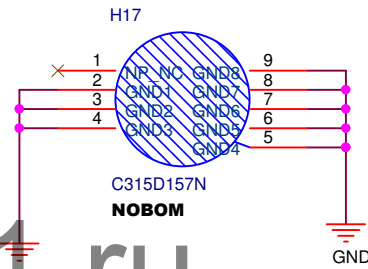
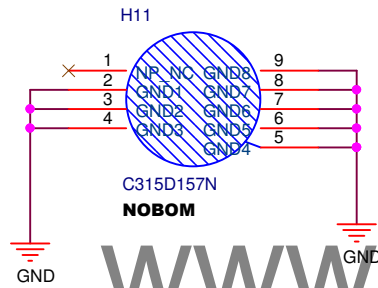
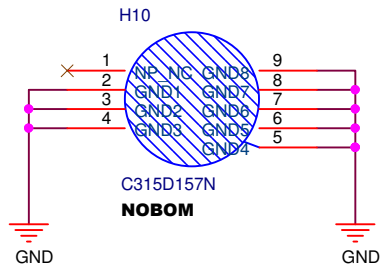
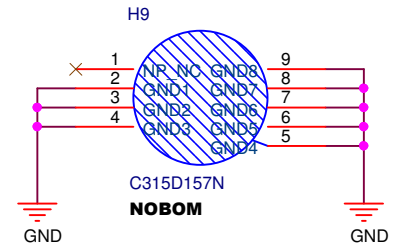
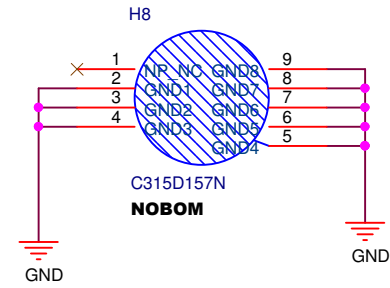
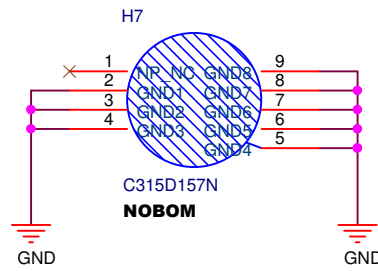
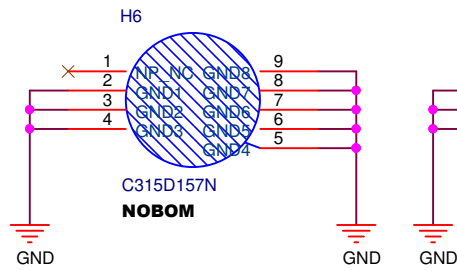
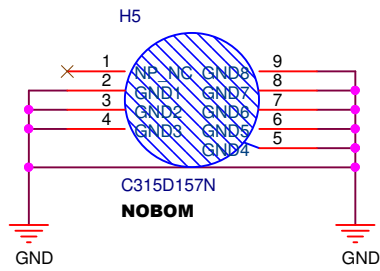
Size A4	Project Name IPMBW-BR	Rev R1.03
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<Core Design>

PEGATRON		Title : 82.SE small card	
PEGATRON CORPORATION		Engineer: CK_Lee	
Size A4	Project Name IPMBW-BR		Rev R1.03
Date: Wednesday, May 13, 2015		Sheet 82	of 85



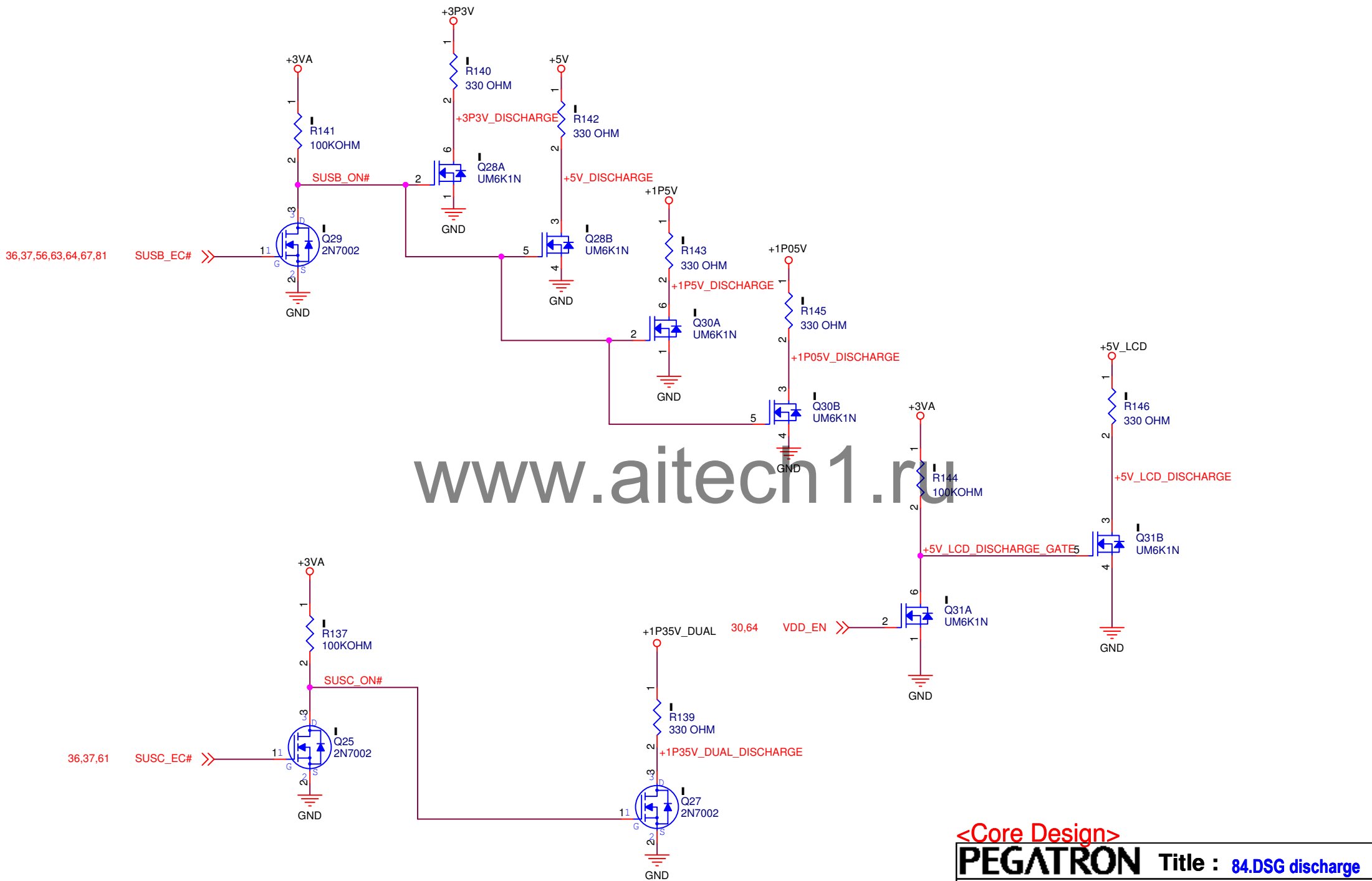
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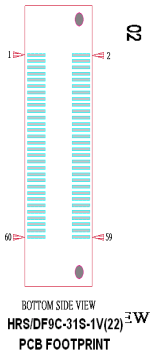
PEGATRON Title : 83.Screw hole

PEGATRON CORPORATION Engineer: CK_Lee

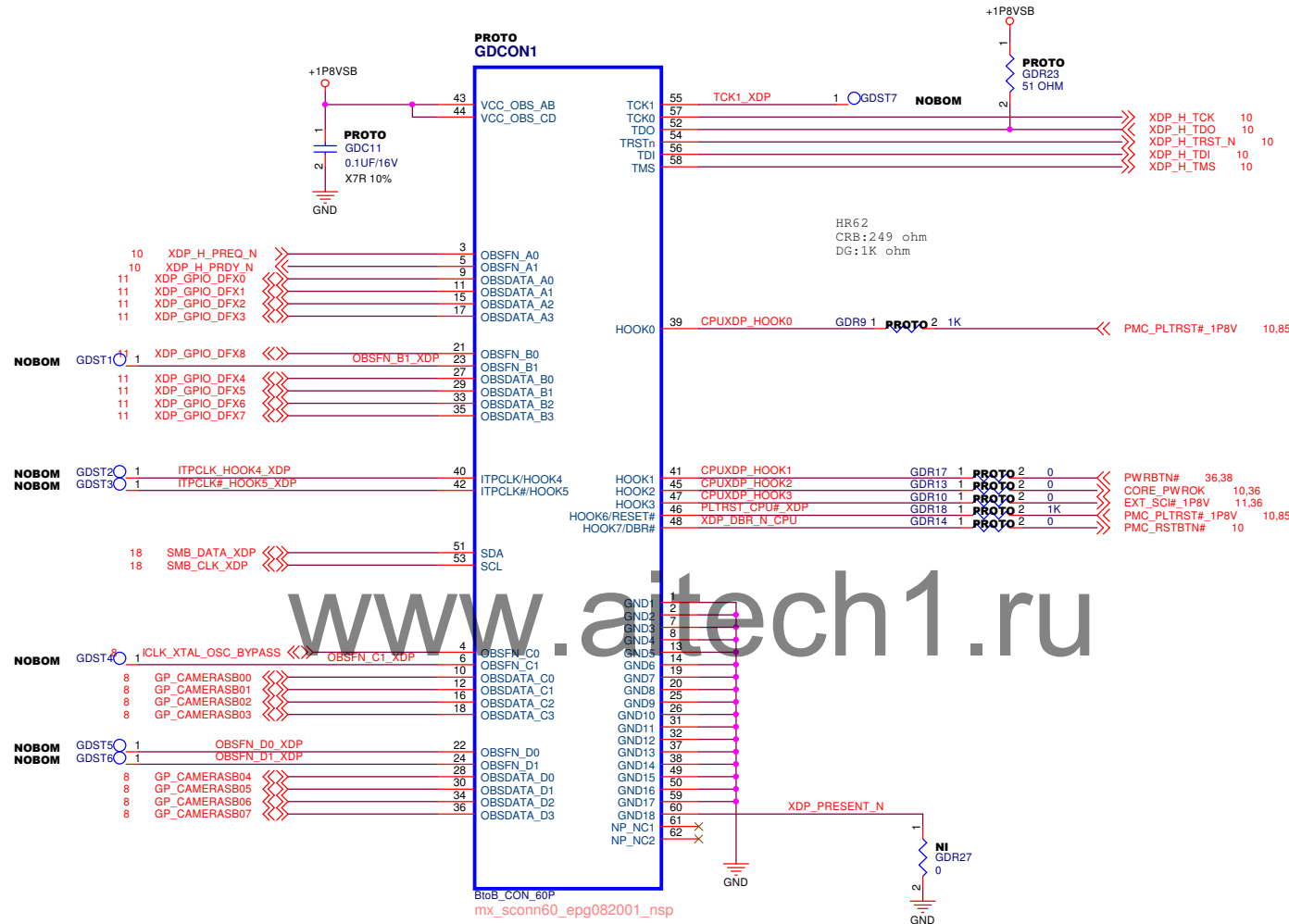
Size	Project Name	Rev
A4	IPMBW-BR	R1.03

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INTEL CPU XDP DEBUG PORT



<Core Design>

PEGATRON		Title : 85.CPU XDP	
PEGATRON CORPORATION		Engineer: CK_Lee	
Size	Project Name	Rev	
A3	IPMBW-BR	R1.03	
Date: Wednesday, May 13, 2015		Sheet	85 of 85